

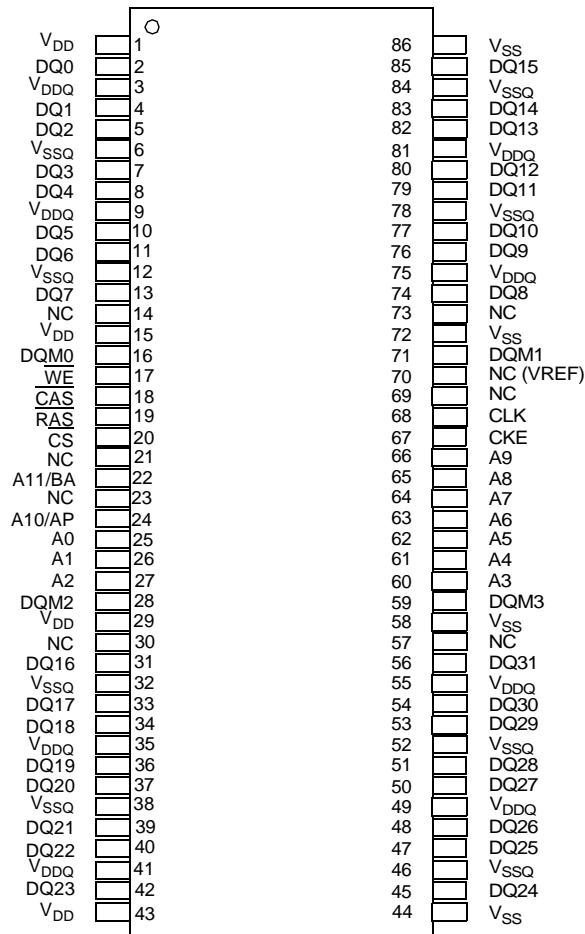
Description

The device is CMOS Synchronous Dynamic RAM organized as 524,288 - word x 32 - bit x 4 - bank, and 1,048,576 - word x 32 - bit x 2 - bank, respectively. It is fabricated with an advanced submicron CMOS technology and designed to operate from a singly 3.3V only power supply. It is packaged in JEDEC standard pinout and standard plastic TSOP package.

Features

- Single 3.3V ($\pm 0.3V$) power supply
- High speed clock cycle time : 8/10 for LVTTL
- High speed clock cycle time : 8/10 for SSTL - 3
- Fully synchronous with all signals referenced to a positive clock edge
- Programmable $\overline{\text{CAS}}$ latency (2,3)
- Programmable burst length (1,2,4,8,& Full page)
- Programmable wrap sequence (Sequential/Interleave)
- Automatic precharge and controlled precharge
- Auto refresh and self refresh modes
- Dual Internal banks controlled by A11 (Bank select) for VG36643211(2)
- Quad Internal banks controlled by A11 & A12 (Bank select) for VG36643241(2)
- Each Banks can operate simultaneously and independently
- LVTTL compatible I/O interface for VG36643211 and VG36643241
- SSTL - 3 compatible I/O interface for VG36643212 and VG36643242
- Random column access in every cycle
- x32 organization
- Input/Output controlled by DQM0 ~ 3
- 4,096 refresh cycles/64ms
- Burst termination by burst stop and precharge command
- Burst read/single write option

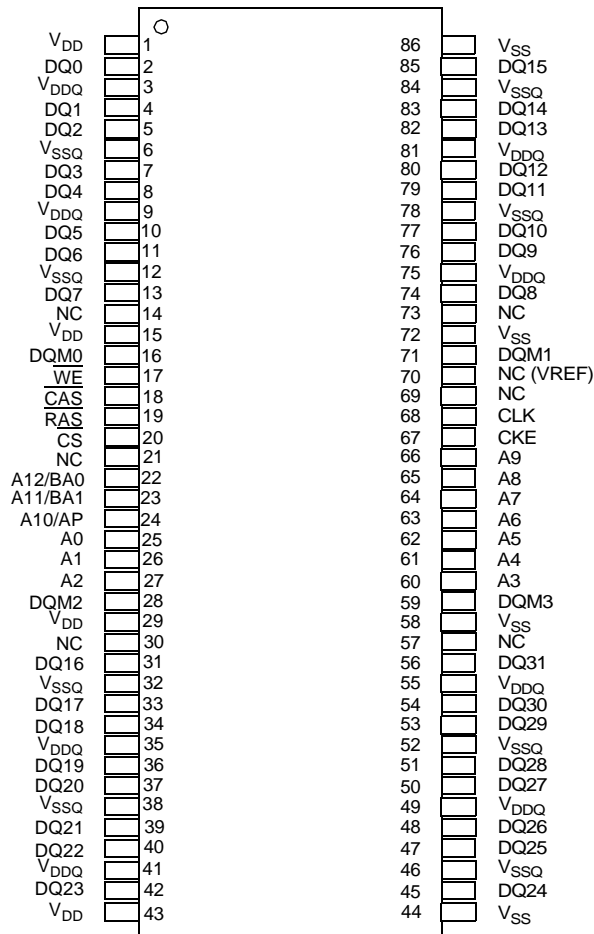
Pin Configuration



Pin Description
VG36643211 (2)

Pin Name	Function	Pin Name	Function
A0 - A11	Address inputs - Row address A0 - A10 - Column address A0 - A8 A11 : Bank select	DQM0 ~ 3	DQ Mask enable
DQ0 ~ DQ31	Data - in/data - out	CLK	Clock input
$\overline{\text{RAS}}$	Row address strobe	CKE	Clock enable
$\overline{\text{CAS}}$	Column address strobe	$\overline{\text{CS}}$	Chip select
$\overline{\text{WE}}$	Write enable	V _{DDQ}	Supply voltage for DQ
V _{SS}	Ground	V _{SSQ}	Ground for DQ
V _{DD}	Power (+ 3.3V)	(V _{REF})	Reference Voltage, SSTL - 3 only

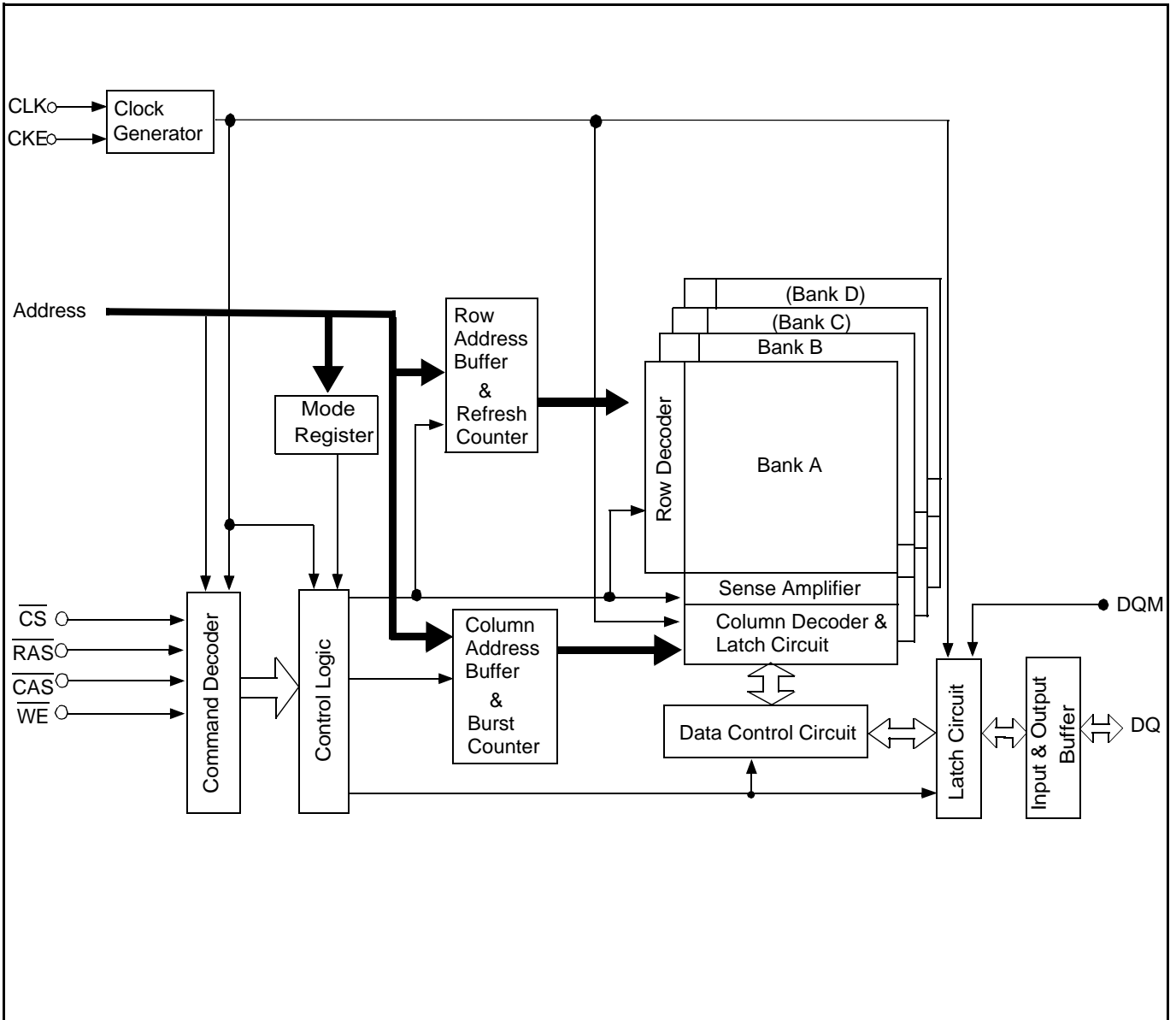
Pin Configuration



Pin Description
VG36643241 (2)

Pin Name	Function	Pin Name	Function
A0 - A12	Address inputs - Row address A0 - A10 - Column address A0 - A7 A11 & A12 : Bank select	DQM0 ~ 3	DQ Mask enable
DQ0 ~ DQ31	Data - in/data - out	CLK	Clock input
$\overline{\text{RAS}}$	Row address strobe	CKE	Clock enable
$\overline{\text{CAS}}$	Column address strobe	$\overline{\text{CS}}$	Chip select
$\overline{\text{WE}}$	Write enable	V _{DDQ}	Supply voltage for DQ
V _{SS}	Ground	V _{SSQ}	Ground for DQ
V _{DD}	Power (+ 3.3V)	(V _{REF})	Reference Voltage, SSTL - 3 only

Block Diagram



Note: Bank C and Bank D are for VG36643241(2) only

Absolute Maximum D.C. Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to + 4.6	V
Supply voltage relative to Vss	V_{DD}, V_{DDQ}	-0.5 to + 4.6	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPT}	0 to + 70	°C
Storage temperature	T_{STG}	-55 to + 125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Maximum A.C. Operating Requirements for LVTTTL Compatible

Parameter	Symbol	Min	Max	Unit	Notes
Input High Voltage	V_{IH}	2.0	$V_{DDQ} + 2.0$	V	2
Input Low Voltage	V_{IL}	$V_{SSQ} - 2.0$	0.8	V	2

Recommended DC Operating Conditions for LVTTTL Compatible

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V
Input High Voltage, all inputs	V_{IH}	2.0	-	$V_{DD} + 0.3$	V
Input Low Voltage, all inputs	V_{IL}	-0.3	-	0.8	V

Recommended DC Operating Conditions for SSTL - 3 Interface

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V
Supply Voltage (Ground)	V_{SS}, V_{SSQ}	0	-	0	V
Reference Voltage	V_{REF}	1.3	1.5	1.7	V
Termination Voltage	V_{TT}	$V_{REF} - 0.05$	V_{REF}	$V_{REF} + 0.05$	V
Input High Voltage, all inputs	$V_{IH(dc)}$	$V_{REF} + 0.2$	-	$V_{DD} + 0.3$	V
Input Low Voltage, all inputs	$V_{IL(dc)}$	-0.3	-	$V_{REF} - 0.2$	V

Capacitance

($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	-	4	pF	1
Input capacitance (all input pins except address pins & data pins.)	C_{I2}	-	4	pF	1
Data input/output capacitance	$C_{I/O}$	-	5	pF	1

Notes : 1. Capacitance measured with effective capacitance measuring method.

2. The overshoot and undershoot voltage duration is $\leq 3\text{ns}$ with no input clamp diodes.

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	VG36648041(2)B						Unit	Notes		
			-8H		-8L		-10					
			Min	Max	Min	Max	Min	Max				
Operating current	I _{CC1}	Burst length = 1 One bank active t _{RC} ≥ t _{RC(MIN.)} , I _o = 0mA	CL = 3		100		100		90	mA	1	
			CL = 2		95		95		85			
Precharge standby current in power down mode	I _{CC 2P}	CKE ≤ V _{IH(MAX.)} , t _{CK} = 15ns			3		3		3	mA		
	I _{CC 2PS}	CKE ≤ V _{IH(MAX.)} , t _{CK} = ∞			2		2		2			
Precharge standby current in Non - power down mode	I _{CC 2N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15ns CS ≥ V _{IH(MIN.)} Input signals are changed one time during 2 CLK cycles.			20		20		20	mA		
	I _{CC 2NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞ CLK ≤ V _{IL(MAX.)} Input signals are stable.			6		6		6			
Active standby current in power down mode	I _{CC 3P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15ns			5		5		5	mA		
	I _{CC 3PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞			4		4		4			
Active standby current in Nonpower down mode	I _{CC 3N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15ns CS ≥ V _{IH(MIN.)} Input signals are changed one time during 2CLKs.			25		25		25	mA		
	I _{CC 3NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞ CLE ≤ V _{IL(MAX.)} Input signals are stable.			10		10		10			
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN.)} I _o = 0mA All banks Active	CL = 3		160		160		135	mA	2	
			CL = 2		145		125		105			
Refresh current	I _{CC5}	t _{RC} = t _{RC(MIN.)}	CL = 3		130		130		110	mA	3,6	
			CL = 2		125		125		105			
Selfrefresh current	I _{CC6}	CKE ≤ 0.2V			2		2		2	mA		
Input leakage current	I _{LI}	V _{in} ≥ 0, V _{in} ≤ V _{DD} + 0.3V Pins not under test = 0V		- 5	5		- 5	5	- 5	5	uA	
Output leakage current	I _{LO}	V _{out} ≥ 0, V _{out} ≤ V _{DD} (MAX) DQ# in H - Z., Dout disabled		- 5	5		- 5	5	- 5	5	uA	
Output Low Voltage	V _{OL}	I _{OL} = 2mA			0.4		0.4		0.4	V	4	
Output High Voltage	V _{OH}	I _{OH} = -2mA		2.4			2.4		2.4	V	4	
Output Low Voltage	V _{OL}	I _{OL} = 16mA			V _{TT} + 0.8		V _{TT} + 0.8		V _{TT} + 0.8	V	5	
Output High Voltage	V _{OH}	I _{OH} = -16mA		V _{TT} + 0.8			V _{TT} + 0.8		V _{TT} + 0.8	V	5	

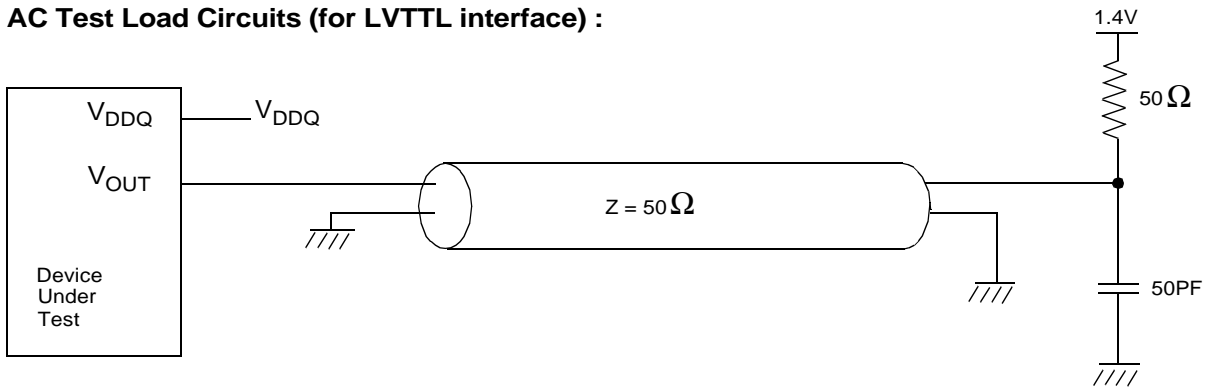
- Notes : 1. ICC1 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, ICC1 is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
2. ICC4 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, ICC4 is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
3. ICC5 is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
4. For LVTTTL compatible, VG3664321(4)1.
5. For SSTL - 3 interface, VG3664321(4)2.
6. Refresh on every 15.6 μs.

A. C Characteristics : (Ta = 0 to 70°C V_{DD} = 3.3V ± 0.3V_{SS} = 0V)

Test Conditions for LVTTTL Compatible :

AC input Levels (V _{IH} /V _{IL})	2.0/0.8V	Input timing reference level/ Output timing reference level	1.4V
Input rise and fall time	1ns	Output load condition	50pF

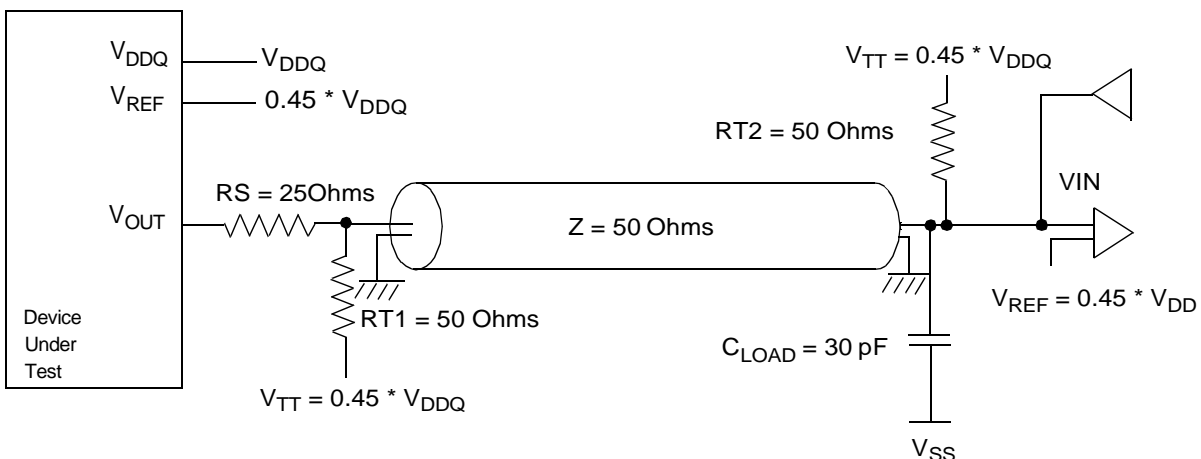
AC Test Load Circuits (for LVTTTL interface) :



Test Conditions for SSTL - 3 Interface

Input High (min)/Input low (max) Voltage	VREF + 0.4V/ VREF - 0.4V	Input Reference Voltage (VREF)	0.45 x VDDQ
Timing Reference Levels of Output Signals	0.45 x VDDQ	Input Signal MAX. Slew Rate	1V/ns
Input Signal MAX. Peak to Peak Swing	2.0V	Output Circuit	See Figure Below
Min. Required output pull - up under AC test load	VTT + 0.8V	Min. Required output pull - down under AC test load	VTT - 0.8V

AC Test Load Circuits (for SSTL - 3 interface) :



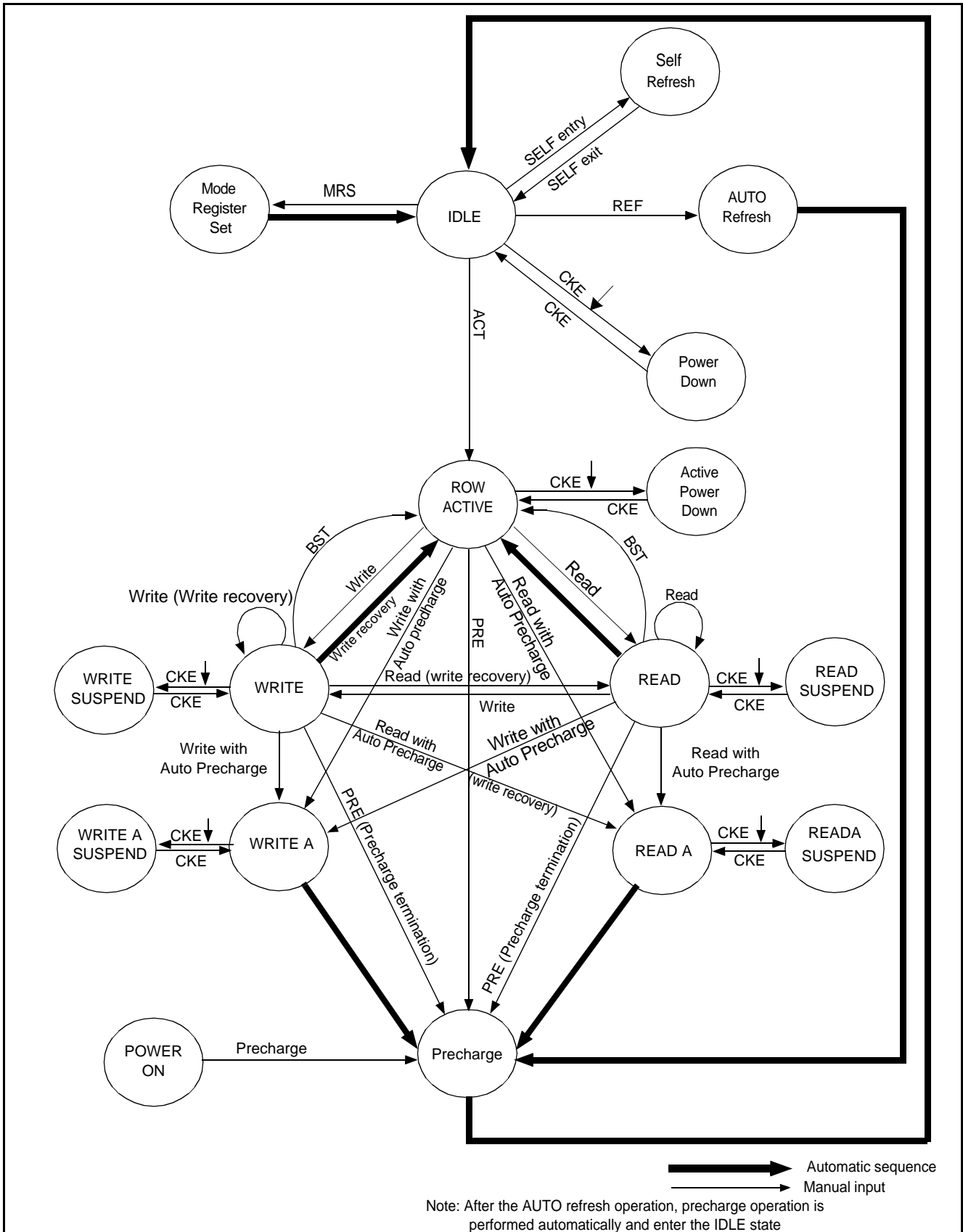
A.C Characteristics : (Ta = 0 to 70°C V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V)

Parameter	CAS Latency	symbol	VG3664321 (4) 1 (2) B						Unit
			-8H		-8L		-10		
			Min	Max	Min	Max	Min	Max	
CLK cycle time ⁽¹⁾	3	t _{ck3}	8		8		10		ns
	2	t _{ck2}	10		12		15		ns
CLK to valid output delay	3	t _{Ac3}		6		6		6	ns
	2	t _{Ac2}		6		6		6	ns
CLK high pulse width		t _{CH}	3		3		3		ns
CLK low pulse width		t _{CL}	3		3		3		ns
CKE setup time		t _{CKS}	2		2		3		ns
CKE hold time		t _{CKH}	1		1		1		ns
Address setup time		t _{AS}	2		2		3		ns
Address hold time		t _{AH}	1		1		1		ns
Command setup time		t _{CMS}	2		2		3		ns
Command hold time		t _{CMH}	1		1		1		ns
Data input setup time		t _{DS}	2		2		3		ns
Data input hold time		t _{DH}	1		1		1		ns
Output data hold time		t _{OH}	3		3		3		ns
CLK to output in low - Z		t _{LZ}	0		0		0		ns
CLK to output in Hi - Z	3	t _{HZ}		6		6		6	ns
	2			6		6		6	
CLK to output in Hi - Z without load		t _{OHN}	1		1		2		ns
Row active to active delay		t _{RRD}	16		16		20		ns
RAS to CAS delay		t _{RCD}	20		20		26		ns
Row precharge time		t _{RP}	20		20		26		ns
ROW active time		t _{RAS}	48	120K	48	120K	60	120K	ns
ROW cycle time		t _{RC}	70		70		90		ns
Last data in to burst stop		t _{BDL}	1		1		1		CLK
Data - in to ACT(REF) command		t _{DAL}	1+ t _{RP}		1+ t _{RP}		1+ t _{RP}		CLK
Data - in to precharge		t _{DPL}	8		8		10		ns
Transition time		t _T ⁽¹⁾	1	10	1	10	1	10	ns
		t _T ⁽²⁾	0.2	5	0.2	5	0.2	5	
Mode reg. set cycle		t _{RSC}	2		2		2		CLK
Self refresh exit time		t _{SRX}	1		1		1		CLK
Refresh time		t _{REF}		64		64		64	ms

Notes : (1) The input clock should be stable and continuous. (jitter ≤ 7% * t_{CK})

Basic Features and Function description

1. simplified State diagram



2. Truth Table

2.1 Command Truth Table

FUNCTION	Symbol	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA ⁽¹⁾	A10	A9 - A0
		n - 1	n							
Device deselect	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	V	H	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Burst stop	BST	H	X	L	H	H	L	X	X	X
CBR (Auto) refresh	REF	H	H	L	L	L	H	X	X	X
Self refresh	SELF	H	L	L	L	L	H	X	X	X

Notes : (1) Bank address. It would be different from organizations.

2.2 DQM Truth Table

FUNCTION	Symbol	CKE		DQM			
		n - 1	n - 1	3	2	1	0
Data write/output enable	ENB	H	X	L			
Data mask/output disable	MASK	H	X	H			
DQ24 ~ DQ31 write enable/output enable	ENB3	H	X	L	X	X	X
DQ16 ~ DQ23 write enable/output enable	ENB2	H	X	X	L	X	X
DQ8 ~ DQ7 write enable/output enable	ENB1	H	X	X	X	L	X
DQ0 ~ DQ7 write enable/output enable	ENB0	H	X	X	X	X	L
DQ24 ~ DQ31 write enable/output enable	MASK3	H	X	H	X	X	X
DQ16 ~ DQ23 write enable/output enable	MASK2	H	X	X	H	X	X
DQ8 ~ DQ15 write enable/output enable	MASK1	H	X	X	X	H	X
DQ0 ~ DQ7 write enable/output enable	MASK0	H	X	X	X		H

2.3 CKE Truth Table

Current State	Function	Symbol	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Add ress
			n - 1	n					
Activating	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	CBR refresh command	REF	H	H	L	L	L	H	X
Idle	Self refresh entry	SELF	H	L	L	L	L	H	X
Self refresh	Self refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power down entry		H	L	X	X	X	X	X
Power down	Power down exit		L	H	X	X	X	X	X

H : High level, L : Low level

X : High or Low level (Don't care), V : Valid Data input

2.4 Operative Command Table Notes 1

(1/3)

Current state	CS	RAS	CAS	WE	Address	Command	Action	Notes
Idle	H	X	X	X	X	DESL	Nop or Power down	2
	L	H	H	X	X	NOP or BST	Nop or Power down	2
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BR, RA	ACT	Row active	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	X	REF/SELF	Refresh or Self refresh	4
	L	L	L	L	Op - Code	MPS	Mode register access	
Row active	H	X	X	X	X	DESL	Nop	
	L	H	H	X	X	NOP or BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read : Determine AP	5
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write : Determine AP	5
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Precharge	6
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue burst to end → Row active	
	L	H	H	H	X	NOP	Continue burst to end → Row active	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, new read : Determine AP	7
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, start write : Determine AP	7,8
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue burst to end → write recovering	
	L	H	H	H	X	NOP	Continue burst to end → write recovering	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, start read : Determine AP	7,8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, new write : Determine AP	7
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	9
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	

Current state	CS	RAS	CA	WE	Address	Command	Action	No
Read with auto precharge	H	X	X	X	X	DESL	Continue burst to end → Precharging	
	L	H	H	H	X	NOP	Continue burst to end → Precharging	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3,11
	L	L	L	H	X	PEF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Write with auto precharge	H	X	X	X	X	DESL	Continue burst to end → write recovering with auto precharge	
	L	H	H	H	X	NOP	Continue burst to end → write recovering with auto precharge	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3,11
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - code	MRS	ILLEGAL	
Precharging	H	X	X	X	X	DESL	Nop → Enter idle after t_{RP}	
	L	H	H	H	X	NOP	Nop → Enter idle after t_{RP}	
	L	H	H	L	X	BST	Nop → Enter idle after t_{RP}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t_{RP}	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Row activating	H	X	X	X	X	DESL	Nop → Enter row active after t_{RCD}	
	L	H	H	H	X	NOP	Nop → Enter row active after t_{RCD}	
	L	H	H	L	X	BST	Nop → Enter row active after t_{RCD}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,9
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	

Current state	\overline{CS}	\overline{RAS}	\overline{CA}	\overline{WE}	Address	Command	Action	Notes
Write recovering	H	X	X	X	X	DESL	Nop → Enter row active after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter row active after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter row active after t_{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	Start read, Determine AP	8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	New write, Determine AP	
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	PEF/SELF	ILLEGAL	
Write recovering with auto precharge	L	L	L	L	Op - Code	MRS	ILLEGAL	
	H	X	X	X	X	DESL	Nop → Enter precharge after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter precharge after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter precharge after t_{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3,8,11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3,11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	REF/PALL	ILLEGAL	3
Auto Refreshing	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
	H	X	X	X	X	DESL	Nop Enter idle after t_{RC}	
	L	H	H	X	X	NOP/BST	Nop Enter idle after t_{RC}	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
Mode register accessing	L	L	H	X	X	ACT/PRE/PALL	ILLEGAL	
	L	L	L	X	X	REF/SELF/MRS	ILLEGAL	
	H	X	X	X	X	DESL	Nop → Enter idle after 2 Clocks	
	L	H	H	H	X	NOP	Nop → Enter idle after 2 Clocks	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRITE	ILLEGAL	
	L	L	X	X	X	ACT/PRE/PALL/REF/SELF/MRS	ILLEGAL	

- Note 1. All entries assume that CKE was active (High level) during the preceding clock cycle.
2. If both banks are idle, and CKE is inactive (Low level), the device will enter Power down mode. All input buffers except CKE will be disabled.
 3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
 4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self refresh mode. All input buffers except CKE will be disabled.
 5. Illegal if t_{RCD} is not satisfied.
 6. Illegal if t_{RAS} is not satisfied.
 7. Must satisfy burst interrupt condition.
 8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
 9. Must mask preceding data which don't satisfy t_{DPL} .
 10. Illegal if t_{RRD} is not satisfied.
 11. Illegal for single bank, but legal for other banks in multi - bank deuleo.

2.5 Command Truth Table for CKE ^{Note 1}

Current state	CKE _{n-1}	CKE _n	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	Address	Action	Notes
Self refresh (S.R.)	H	X	X	X	X	X	X	INVALID, CLK (n - 1) would exit S.R.	
	L	H	H	X	X	X	X	S.R. Recovery	2
	L	H	L	H	H	X	X	S.R. Recovery	2
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	Maintain S.R.	
Self refresh recovery	H	H	H	X	X	X	X	Idle after t _{RC}	
	H	H	L	H	H	X	X	Idle after t _{RC}	
	H	H	L	H	L	X	X	ILLEGAL	
	H	H	L	L	X	X	X	ILLEGAL	
	H	L	H	X	X	X	X	Begin clock suspend next cycle	5
	H	L	L	H	H	X	X	Begin clock suspend next cycle	5
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	H	X	X	X	X	X	Exit clock suspend next cycle	2
L	L	X	X	X	X	X	Maintain clock suspend		
Power down (P.D.)	H	X	X	X	X	X		INVALID, CLK (n - 1) would exit P.D.	
	L	H	X	X	X	X	X	EXIT P.D. → Idle	2
	L	L	X	X	X	X	X	Maintain power down mode	
Both banks idle	H	H	H	X	X	X		Refer to operations in Operative Command Table	
	H	H	L	H	X	X		Refer to operations in Operative Command Table	
	H	H	L	L	H	X		Refer to operation in Operative Command Table	
	H	H	L	L	L	H	X	Auto Refresh	
	H	H	L	L	L	L	Op - Code	Refer to operations in Operative Command Table	
	H	L	H	X	X	X		Refer to operations in Operative Command Table	
	H	L	L	H	X	X		Refer to operations in Operative Command Table	
	H	L	L	L	H	X		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	X	Self refresh	3
	H	L	L	L	L	L	Op - Code	Refer to operations in Operative Command Table	
	L	X	X	X	X	X	X	Power down	3
Any state other than listed above	H	H	X	X	X	X	X	Refer to operations in Operative Command Table	
	H	L	X	X	X	X	X	Begin clock suspend next cycle	4
	L	H	X	X	X	X	X	Exit clock suspend next cycle	
	L	L	X	X	X	X	X	Maintain clock suspend	

- Note 1. H : High level, L : low level, X : High or low level (Don't care).
 2. CKE Low to High transition will re - enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
 3. Power down and Self refresh can be entered only from the both banks idle state.
 4. Must be legal command as defined in Operative Command Table.
 5. Illegal if t_{SREX} is not satisfied.

5.Mode Register (Address Input for Mode Set)

13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	Reserved						

JEDEC Standard Test Set

13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	1	0	0	LTMODE	WT	BL				

Burst Read and Single Write (for Write Through Cache)

13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	0	0	0	LTMODE	WT	BL				

Burst Read and Burst Write

X = Don't care

Burst length	Bits2 - 0	WT = 0	WT = 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
111	Full page	R	

Wrap type	0	Sequential
	1	Interleave

Latency mode	Bits6 - 4	CAS latency
	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
111	R	

Remark R : Reserved

5.1 Burst Length and Sequence

(Burst of Two)

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

(Burst of Four)

Starting Address (column address A1 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

(Burst of Eight)

Starting Address (column address A2 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence(decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of sequential addressing, with the length being 256 for 4B 2M x 32, and 512 for 2B 2M x 32.

6.Address Bits of Bank-Select and Precharge

6.1 Qual banks controlled by A11 (for VG36643211/VG36643212)

Row	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	0	Select Bank A "Activate" command
(Activate command)													1	Select Bank B "Activate" command

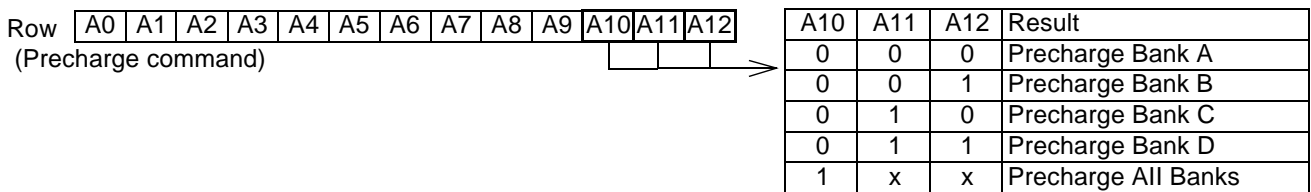
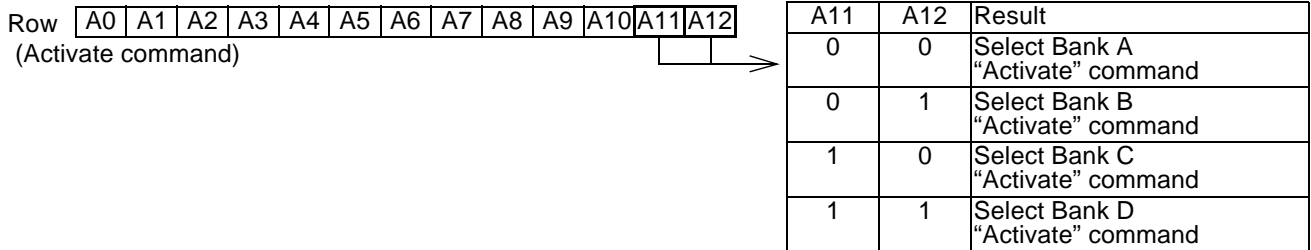
Row	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A10	A11	Result
(Activate command)													0	0	Precharge Bank A
													0	1	Precharge Bank B
													1	X	Precharge All Banks

X : Don't care

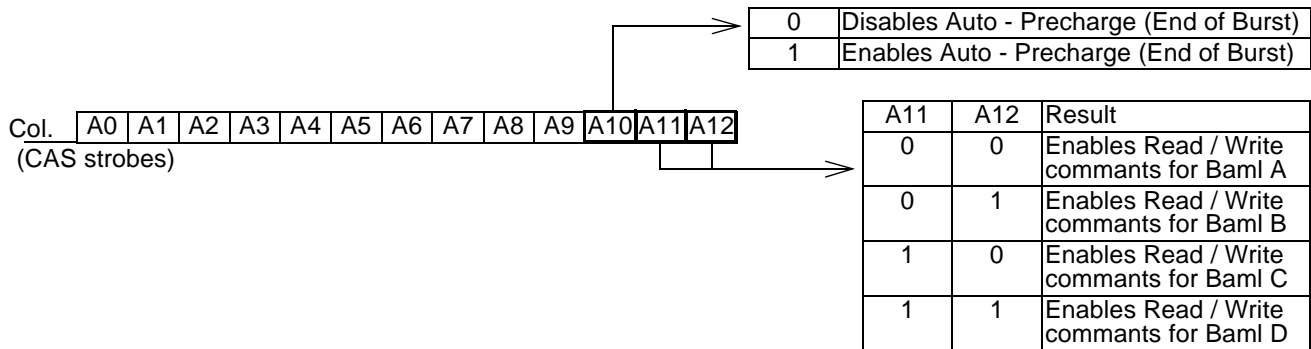
													0	disables Auto - Precharge (End of Burst)
													1	Enables Auto - Precharge (End of Burst)

Co1	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	0	enables Read / Write commands for Bank B
(CAS strobes)													1	enables Read / Write commands for Bank B

6.2 Quad banks controlled by A11 & A12 (for VG36643241 / VG36643242)



X : Don't care



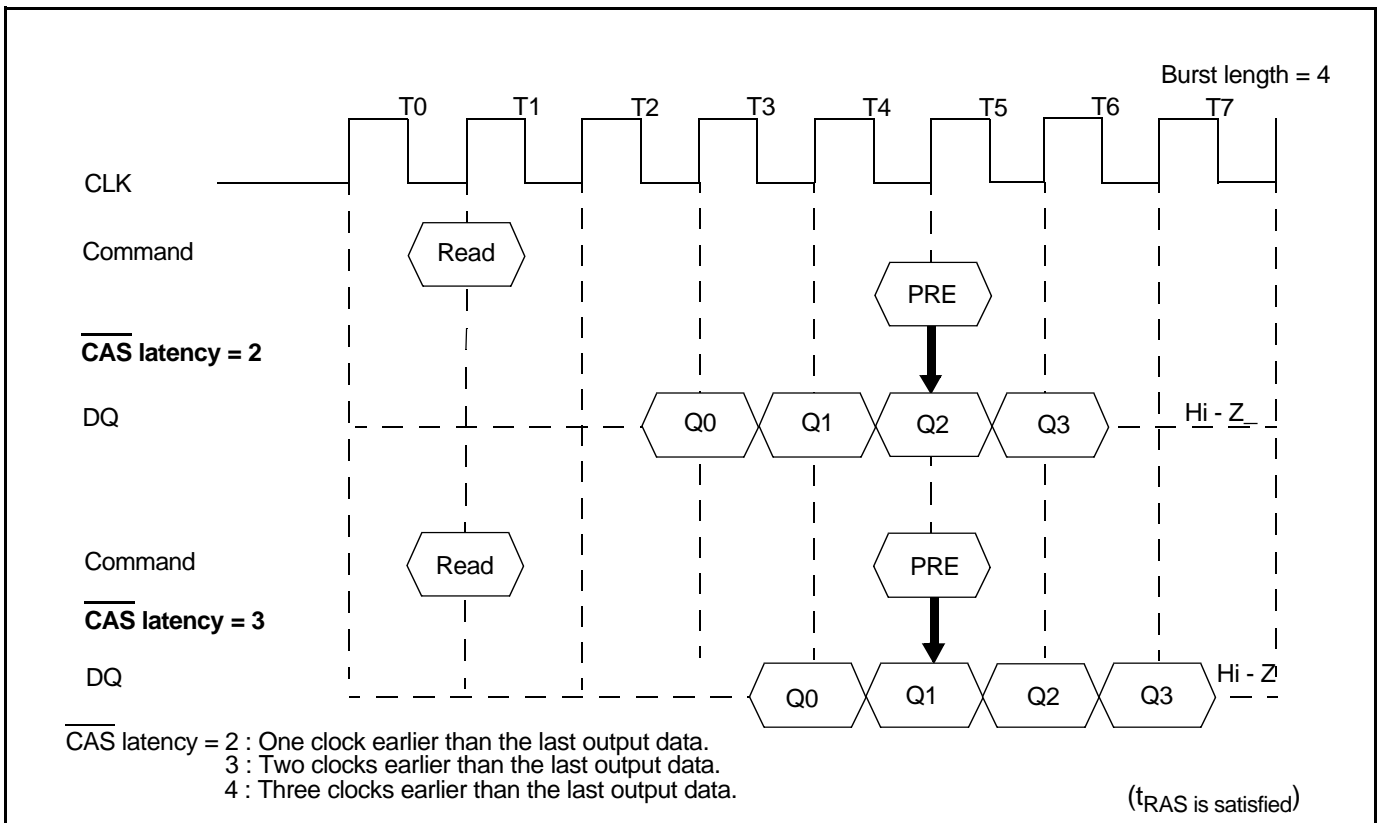
7.PRECHARGE

The precharge command can be asserted anytime after $t_{RAS(min)}$ is satisfied.

Soon after the precharge command is asserted, the precharge operation is performed and the synchronous DRAM enters the idle state after $t_{RP(min)}$ is satisfied. The parameter t_{RP} is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be asserted without losing any data in the burst is as follows.

PRECHARGE



In order to write all data to the memory cell correctly, the asynchronous parameter " t_{DPL} " must be satisfied. The $t_{DPL(min)}$ specification defines the earliest time that a precharge command can be asserted. The minimum number of clocks are calculated by dividing $t_{DPL(min)}$ by the clock cycle time.

In summary, the precharge command can be asserted relative to reference clock that indicates the last data word is valid. In following table, minus means clocks before the reference; plus means time after the reference.

CAS latency	Read	Write
2	-1	+ $t_{DPL(min)}$
3	-2	+ $t_{DPL(min)}$

8.Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. If A10 is high in the read or write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and precharging begins automatically after the burst access.

In the write cycle, $t_{DAL(min.)}$ must be satisfied before asserting the next activate command to the bank being precharged.

When using auto precharge in the read cycle, knowing when the precharge starts is important because the next activate command to the bank being precharged cannot be executed until the precharge cycle ends. Once auto precharge has started, an activate command to the bank can be asserted after t_{RP} has been satisfied.

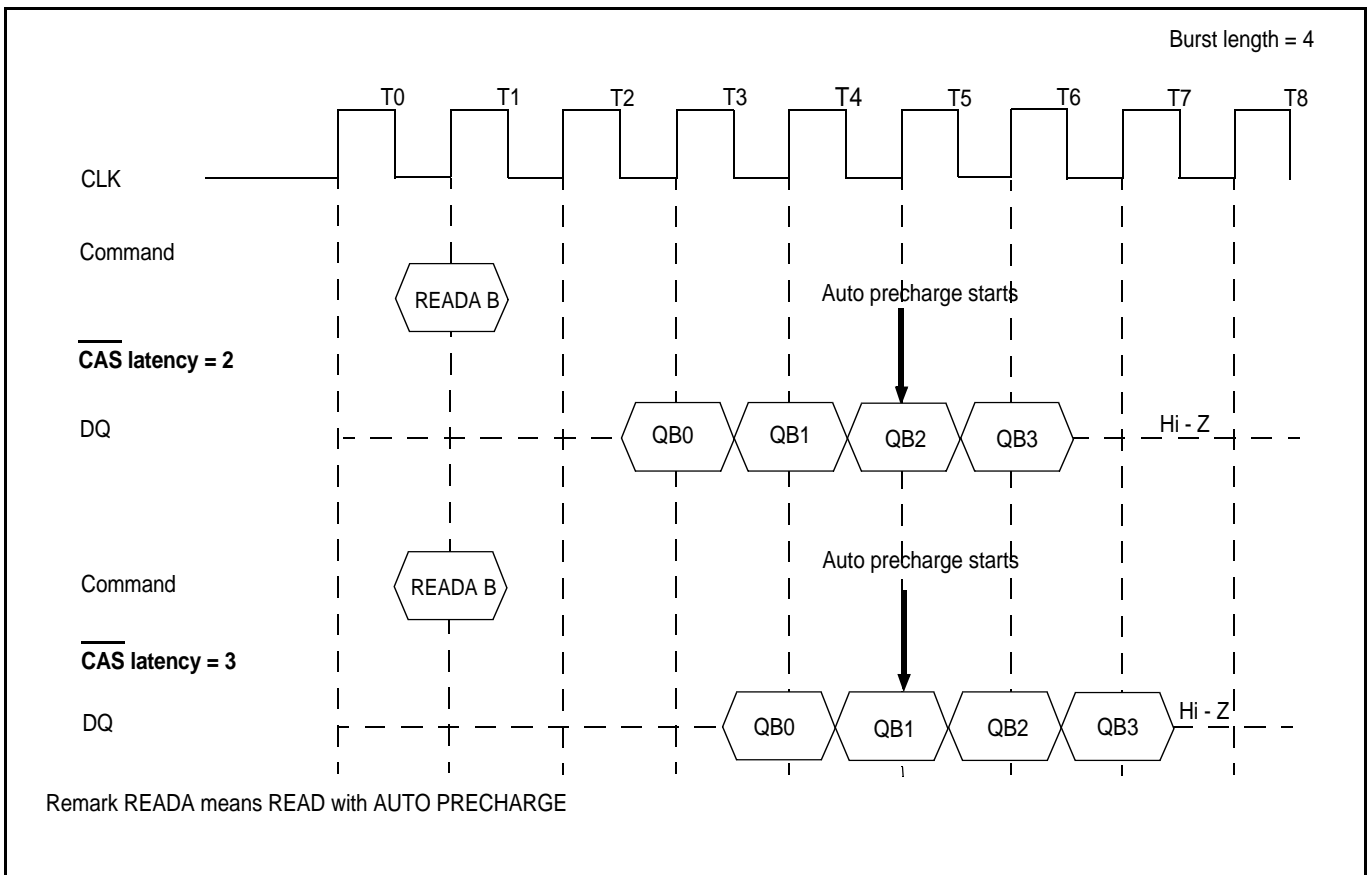
A Read or Write command without auto - precharge can be terminated in the midst of a burst operation. However, a Read or Write command with auto - precharge can not be interrupted by the same bank commands before the entire burst operation is completed. Therefore use of the same bank Read, Write, Precharge or Burst Stop command is prohibited during a read or write cycle with auto - precharge. It should be noted that the device will not respond to the Auto - Precharge command if the device is programmed for full page burst read or write cycles.

The timing when the auto precharge cycle begins depends both on both the \overline{CAS} latency programmed into the mode register and whether the cycle is read or write.

8.1 Read with Auto Precharge

During a READA cycle, the auto precharge begins one clock earlier (CL = 2) or two clocks earlier (CL = 3) than the last word output.

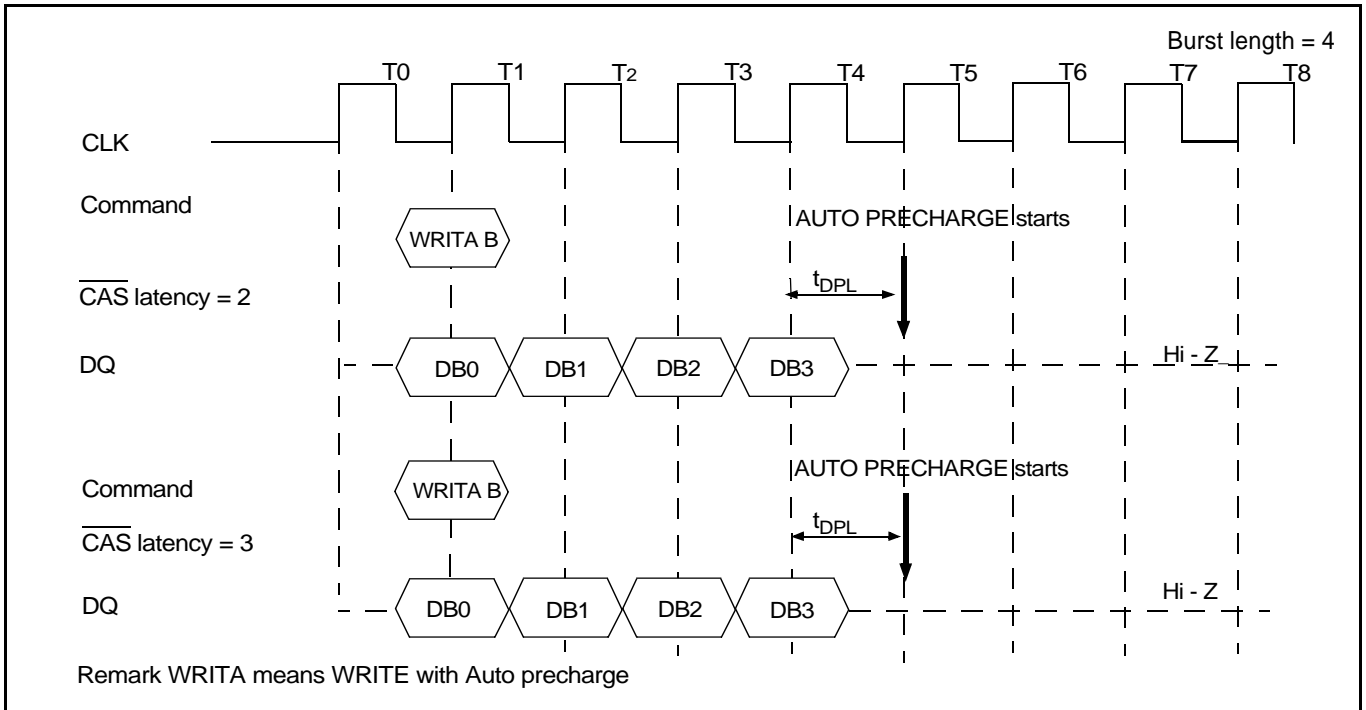
READ with AUTO PRECHARGE



8.2 Write with Auto Precharge

During a write cycle, the auto precharge starts at the timing that is equal to the value of $t_{DPL(min.)}$ after the last data word input to the device.

WRITE with AUTO PRECHARGE



In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid.

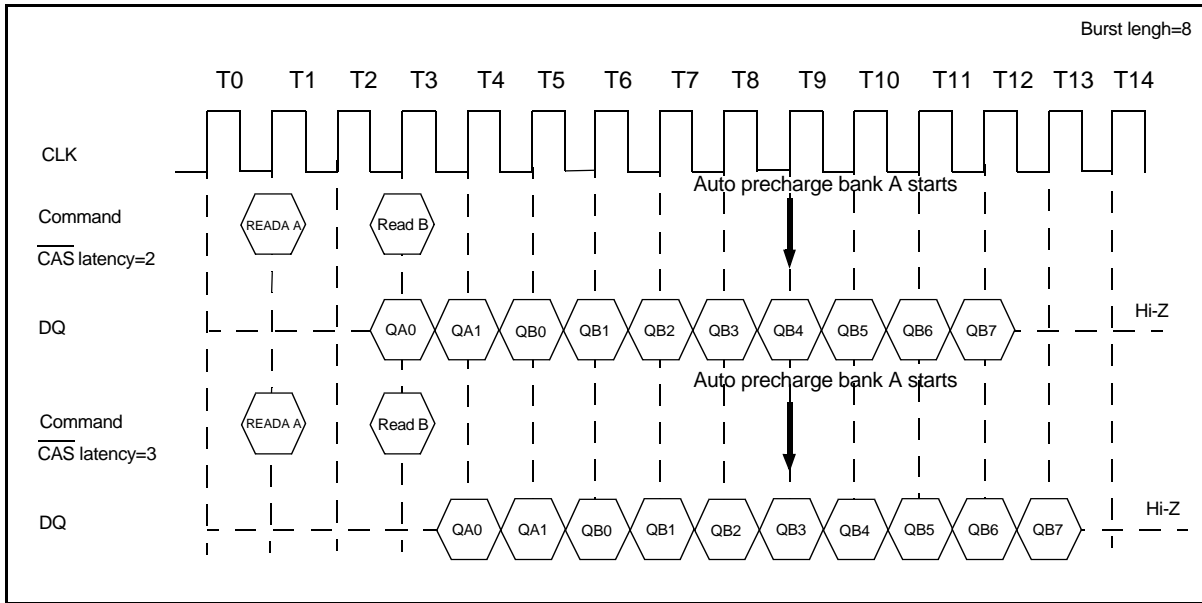
In the table below, minus means clocks before the reference; plus means clocks after the reference.

CAS latency	Read	Write
2	-1	+ $t_{DPL(min.)}$
3	-2	+ $t_{DPL(min.)}$

8.3 Multidank Operation - Read with Auto Precharge

During a READA cycle interrupted by a Read. Write command of another banks, the auto - precharge scheduled time would not be changed.

Multibank Operation

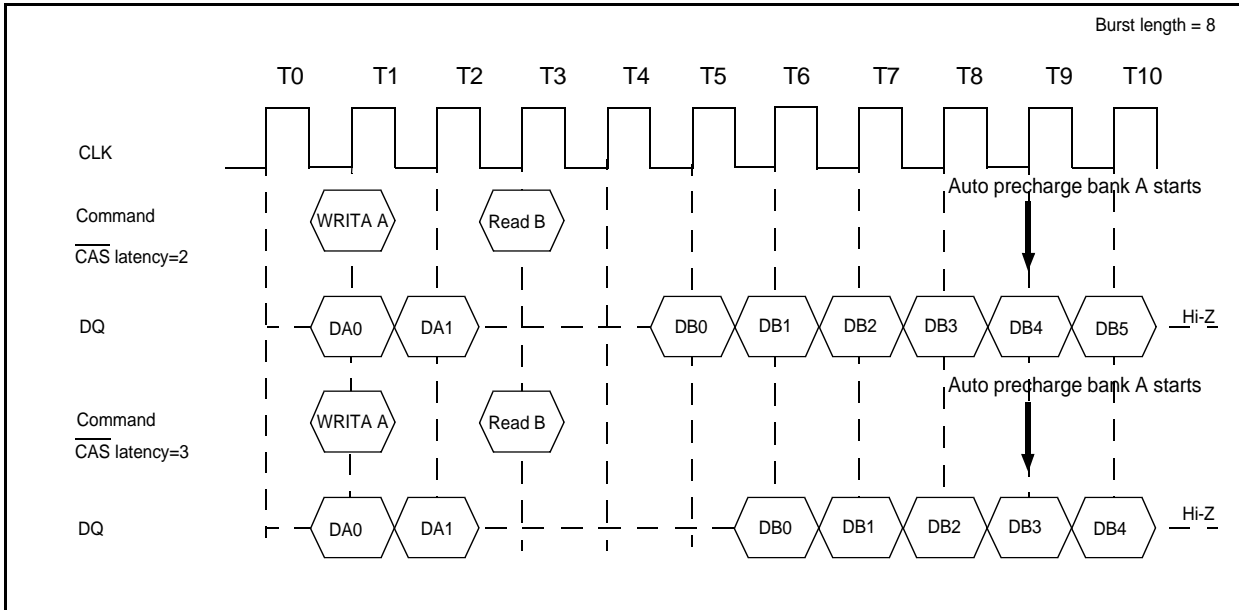


similar top. 21

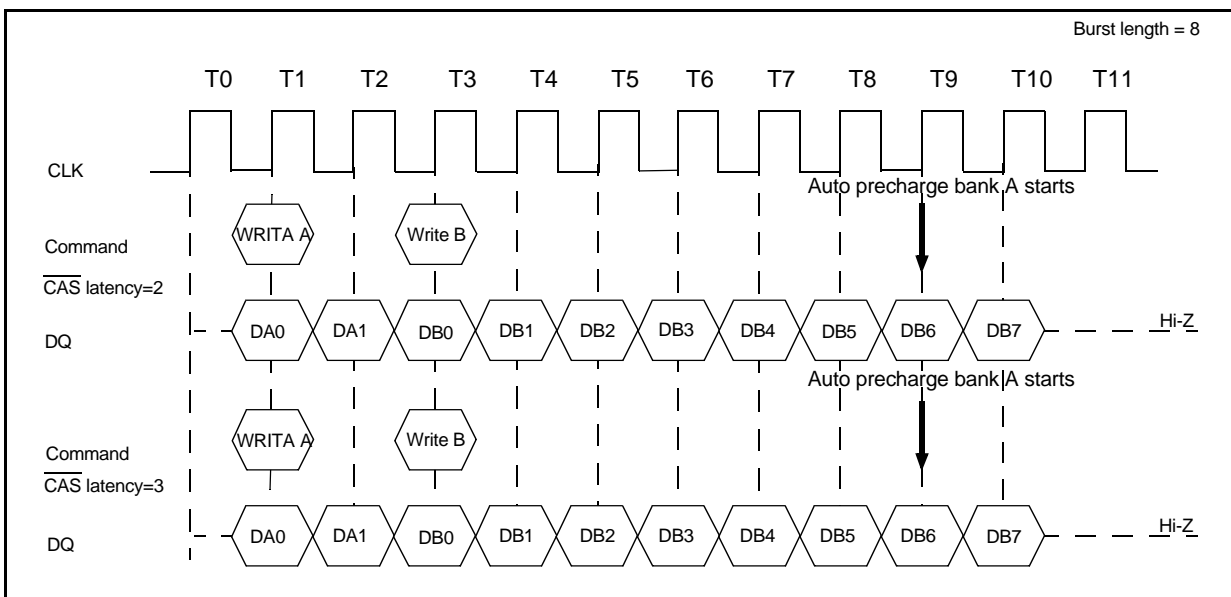
8.3 Multidank Operation - Write with Auto Precharge

During a WRITEA cycle interrupted by a Read, Write command of another banks, the auto - precharge scheduled time would not be changed.

Multidank Operation



Multibank Operation



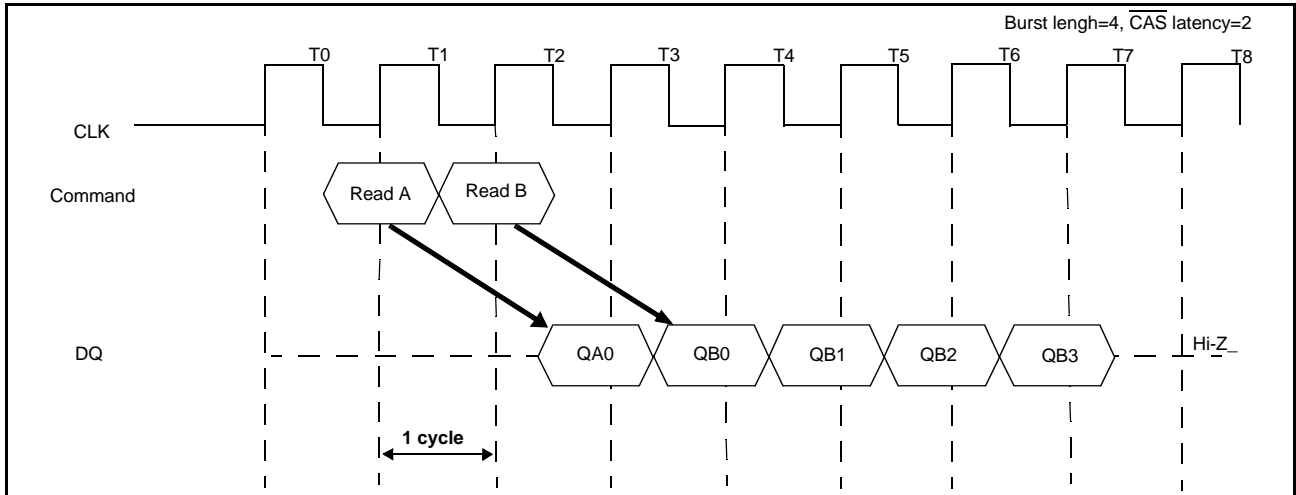
9.READ/WRITE Command Interval

9.1 Read to Read command interval

During a read cycle when a new read command is asserted, it will be effective after the $\overline{\text{CAS}}$ latency, even if the previous read operation has not completed. READ will be interrupted by another READ.

Each read command can be asserted in every clock without any restriction.

READ to READ Command Interval

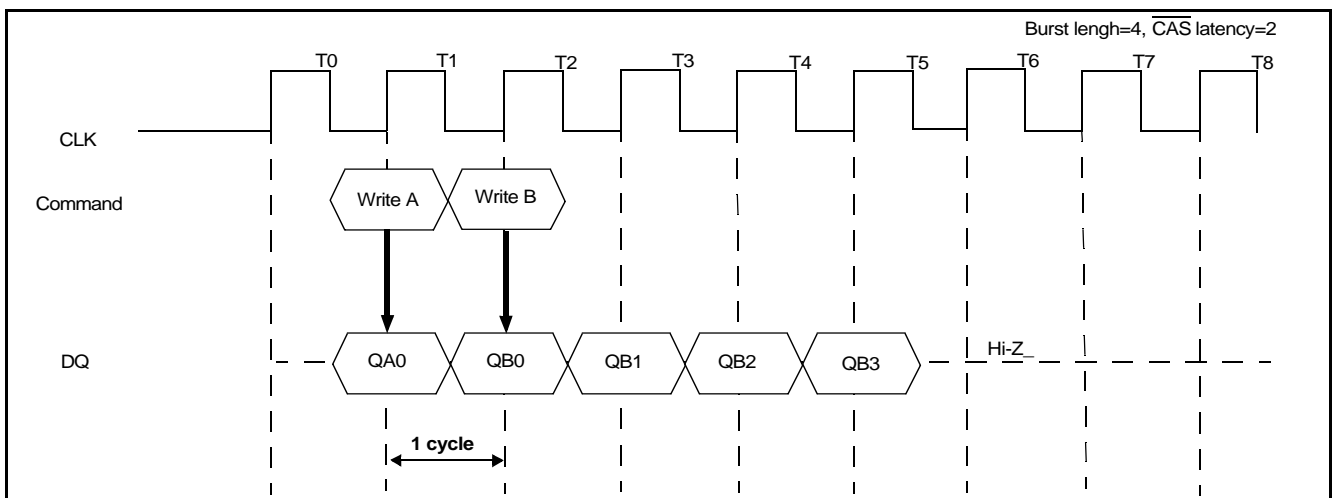


9.2 WRITE to WRITE Command Interval

During a write cycle, when a new Write command is asserted, the previous burst will be terminated and the new burst will begin with a new write command. WRITE will be interrupted by another WRITE.

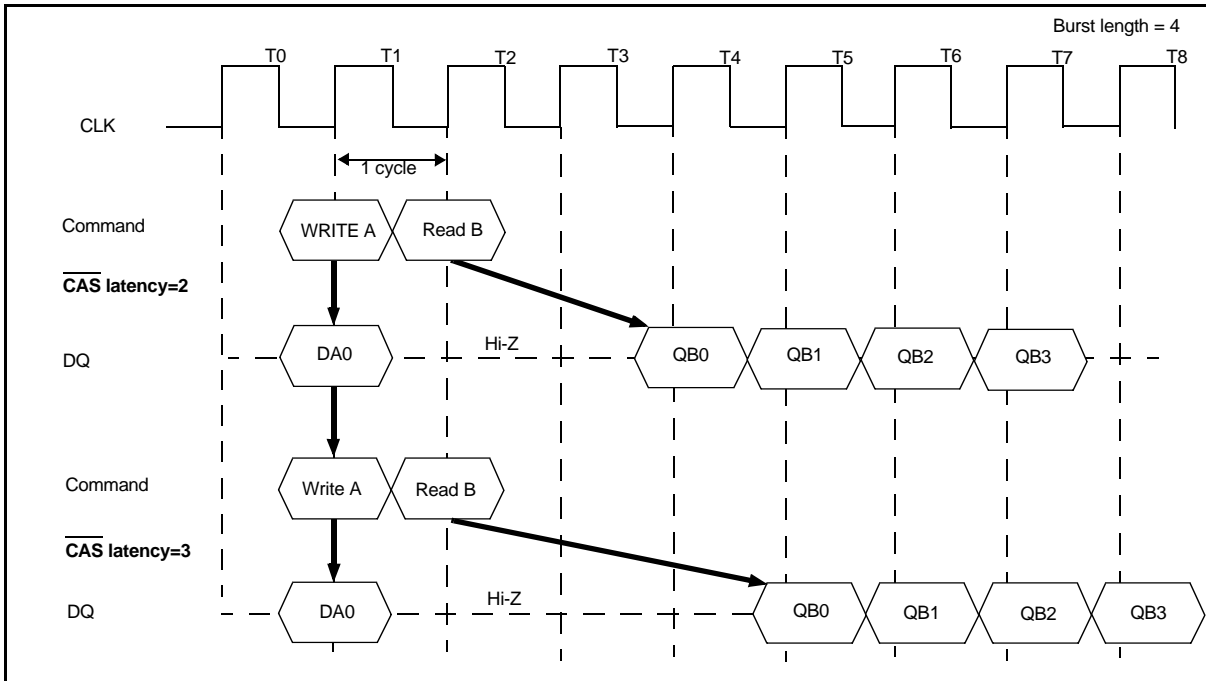
Each write command can be asserted in every clock without any restriction.

WRITE to WRITE Command Interval



9.3 Write to Read Command Interval

The write command to read command to read command interval is also a minimum of 1 cycle. Only the write data before the read command will be written. The data bus must be Hi - Z at least one cycle prior to the first D_{OUT}.



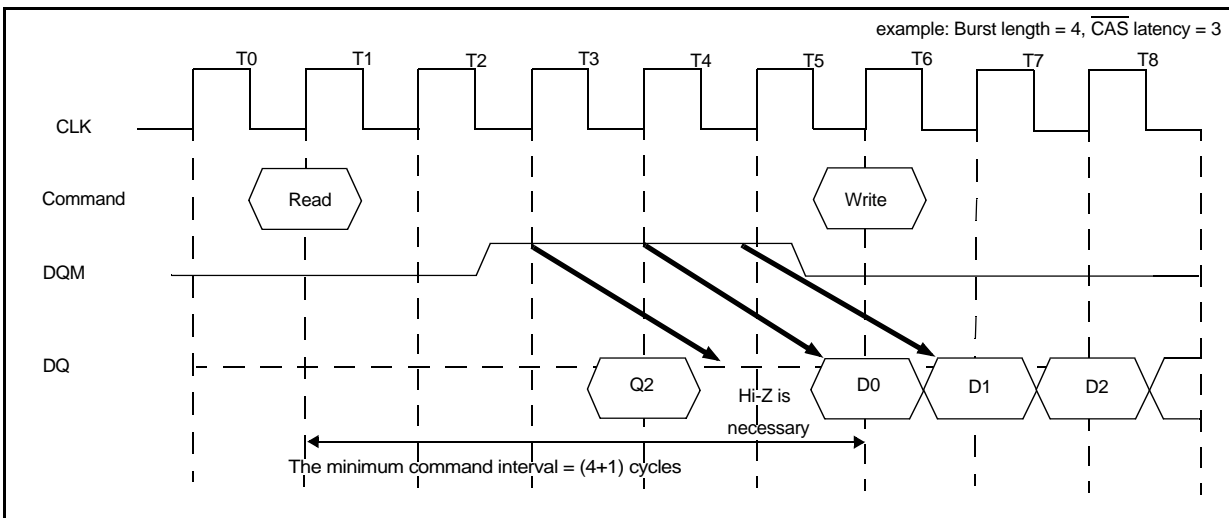
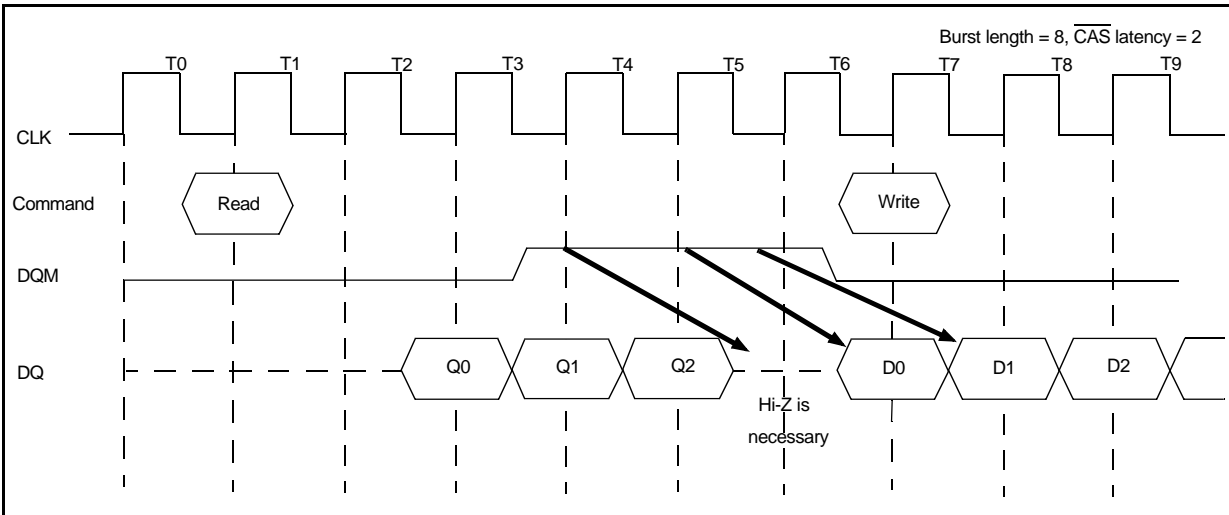
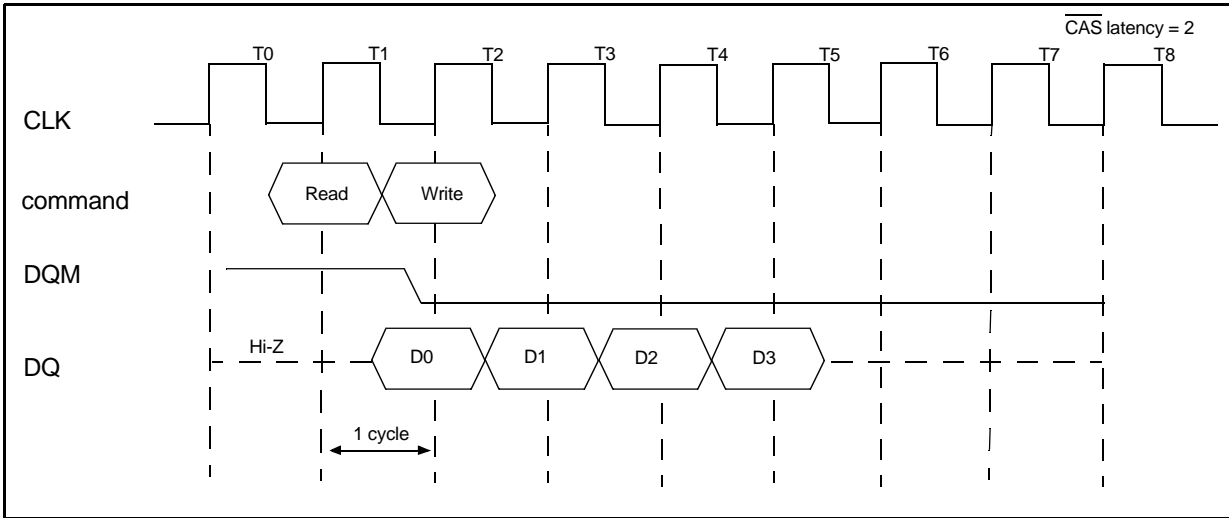
9.4 Read to Write command Interval

During READ cycle, READ can be interrupted by WRITE. When the CAS latency is 3 and the burst length is Full page, the burst read cannot be interrupted by WRITE (A Burst Stop command (BST) or a - Precharge command can interrupt).

In case CAS latency is 2, the read and write command interval is 1 cycle minimum. The data bus must be Hi - Z using DQM before WRITE and DQM must be High at least 3 clocks prior to the Write command. There is a restriction to avoid data conflict.

In case CAS latency is 3 (burst length is not Full page), READ can be interrupted by WRITE command. The minimum command interval is [burst length + 1] cycles. DQM must be High at least 3 clocks prior to the Write command.

READ to WRITE Command Interval



10. Burst Termination

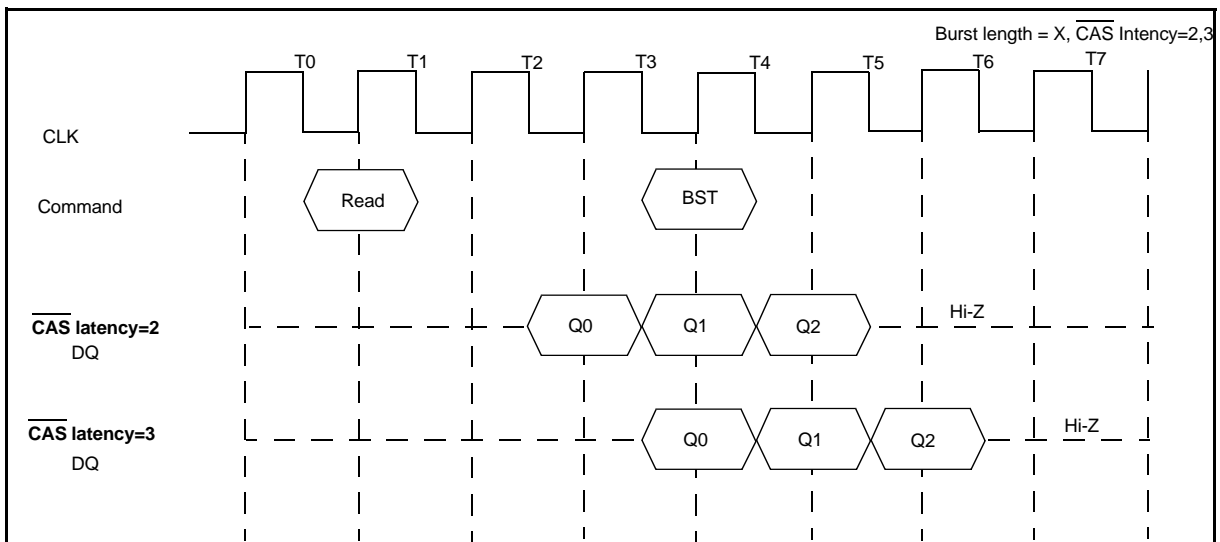
There are two methods to terminate a burst operation other than using a read or a write command. One is the burst stop command and the other is the precharge command.

10.1 Burst Stop Command

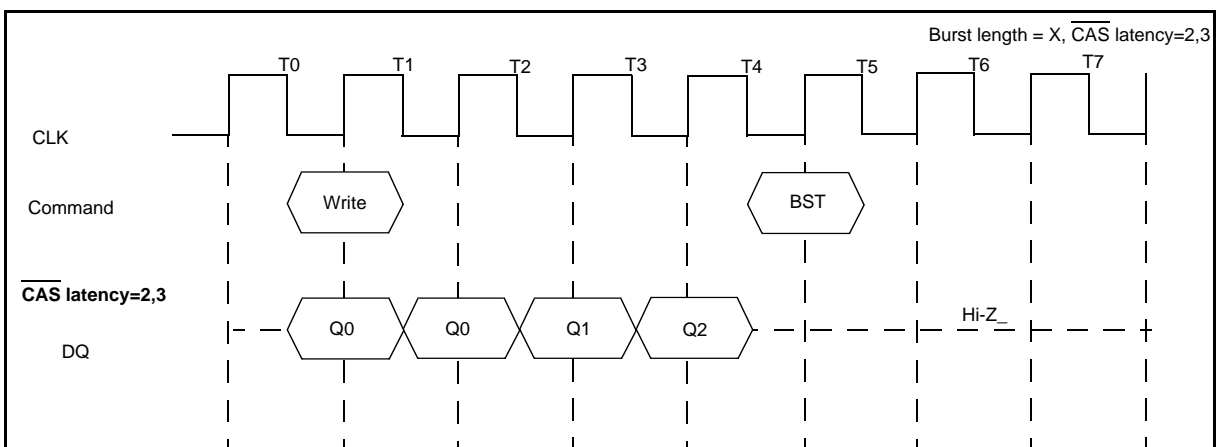
During a read burst, when the burst stop command is asserted, the burst read data are terminated and the data bus goes to high - impedance after the $\overline{\text{CAS}}$ latency from the burst stop command.

During a write burst, when the burst stop command is asserted, any data provided at that cycle will not be written. The burst write is effectively terminated and no further data can be written until a new write command is asserted.

Burst Termination



Remark BST : Burst stop command



Remark BST : Burst stop command

10.2 Precharge Termination

10.2.1

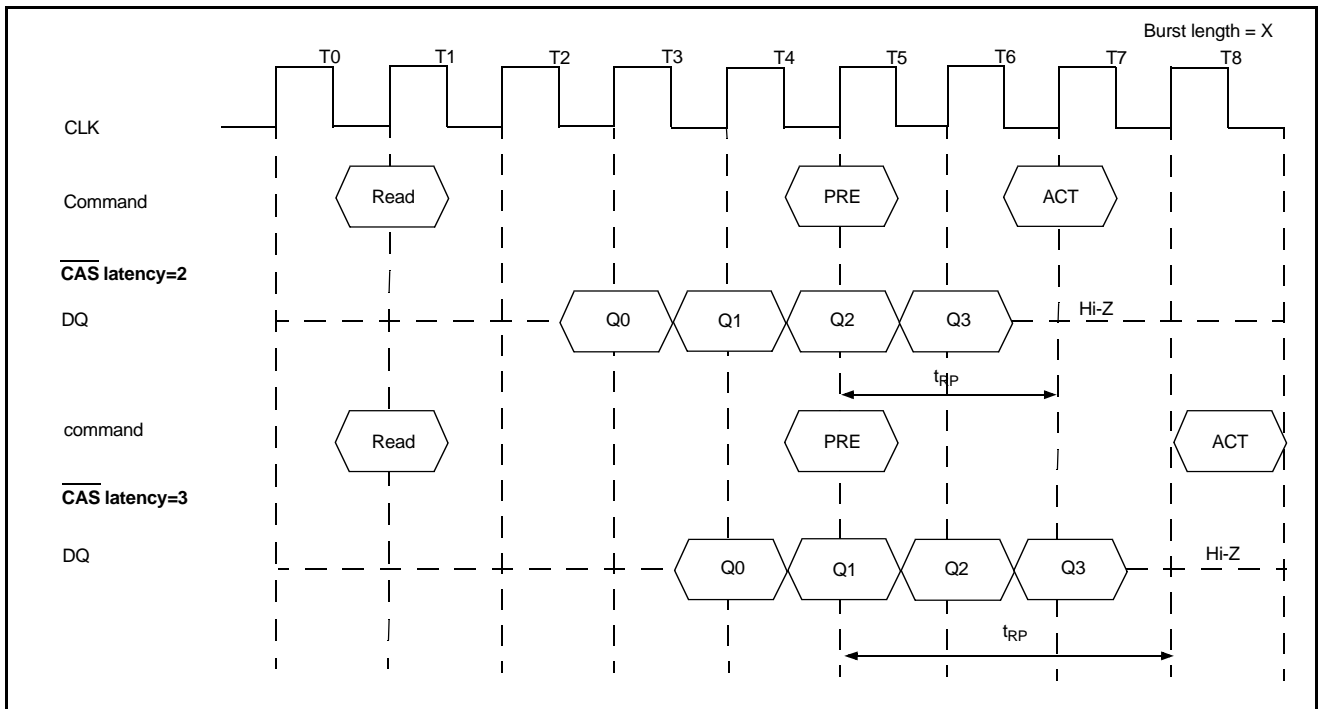
During READ cycle, the burst read operation is terminated by a precharge command. When the precharge command is asserted, the burst read operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command.

When $\overline{\text{CAS}}$ latency is 2, the read data will remain valid until one clock after the precharge command.

When $\overline{\text{CAS}}$ latency is 3, the read data will remain valid until two clocks after the precharge command.

Precharge Termination in READ Cycle



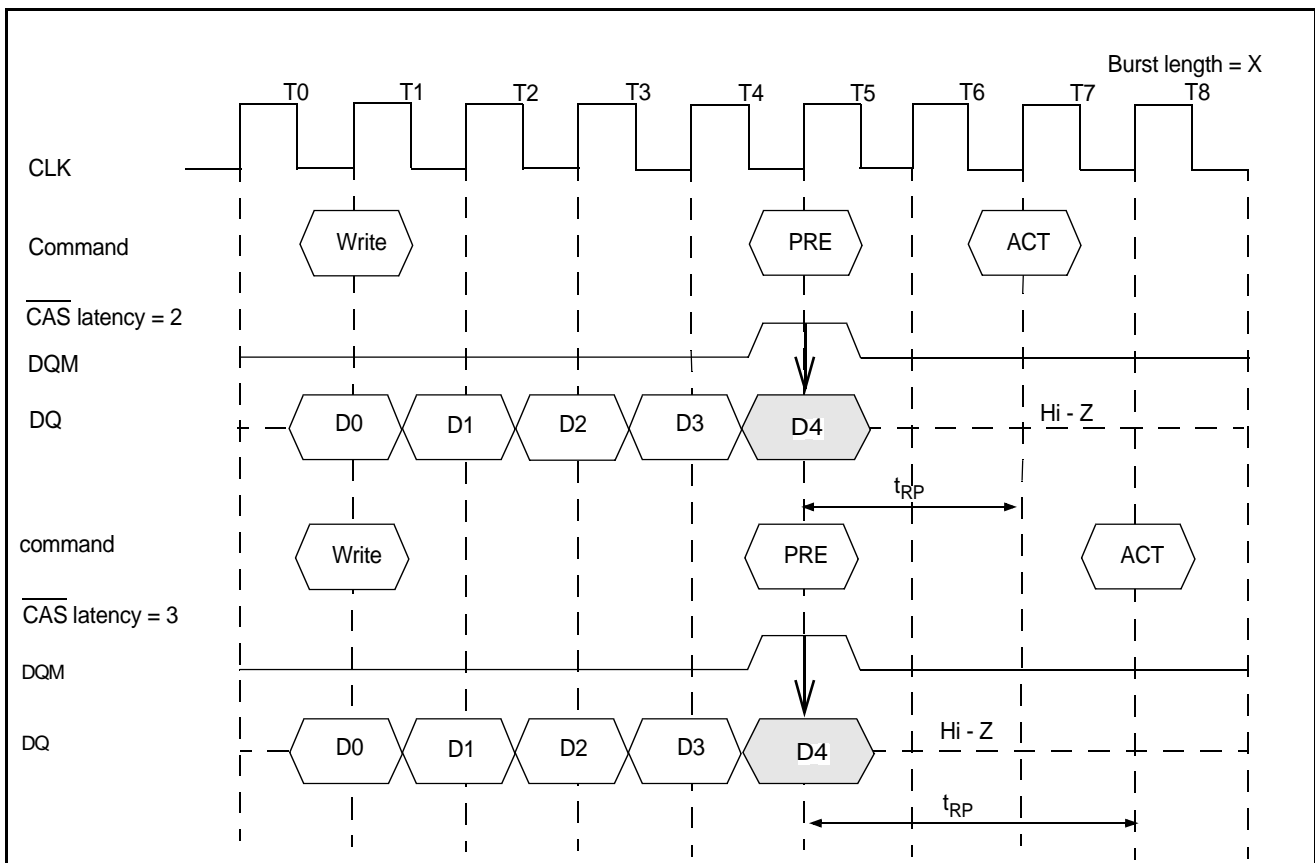
10.2.2 Precharge Termination in WRITE Cycle

During WRITE cycle, the burst write operation is terminated by a precharge command. When the precharge command is asserted, the burst write operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command. The DQM must be high to mask invalid data in.

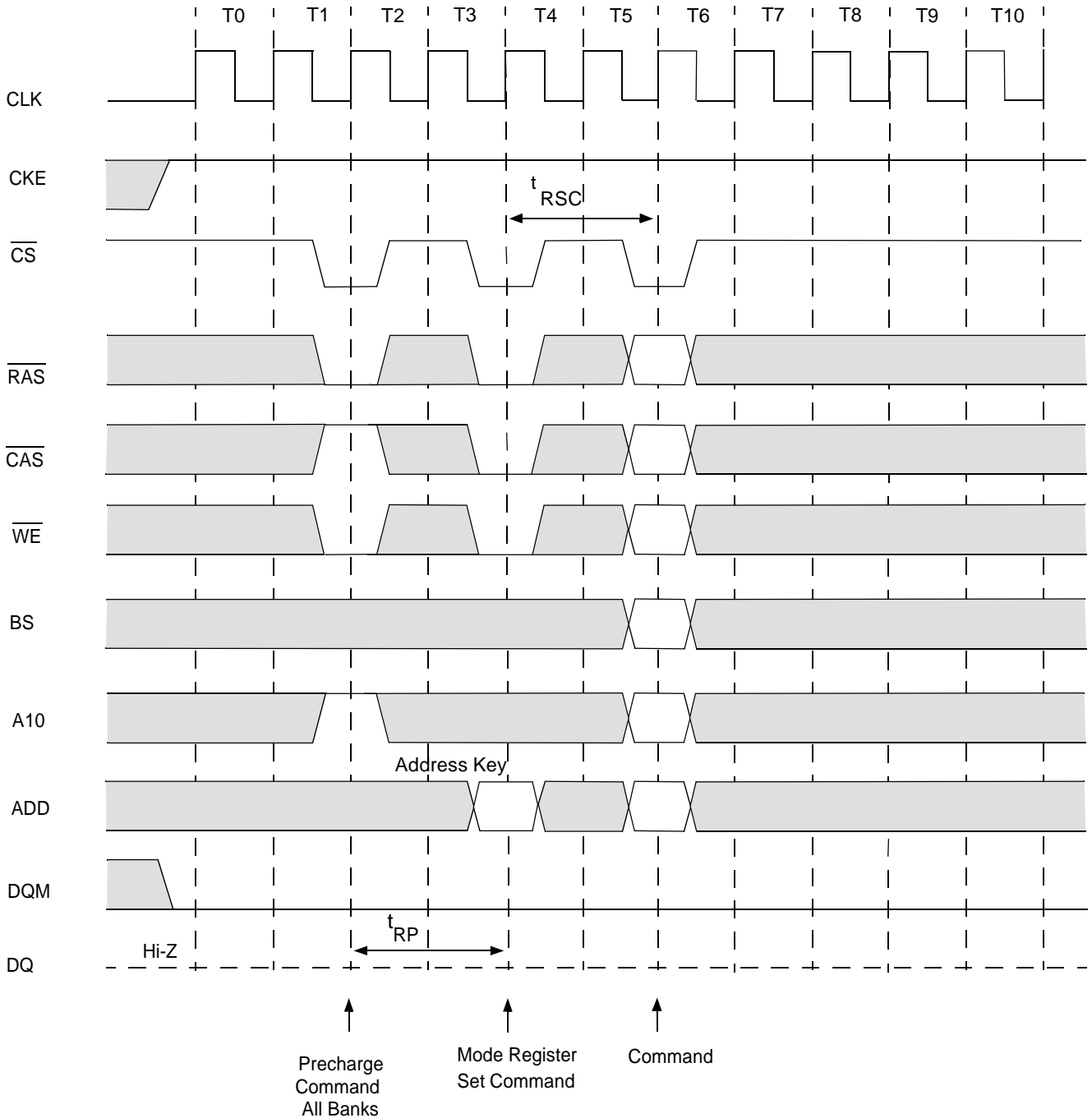
When CAS latency is 2, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.

When CAS latency is 3, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



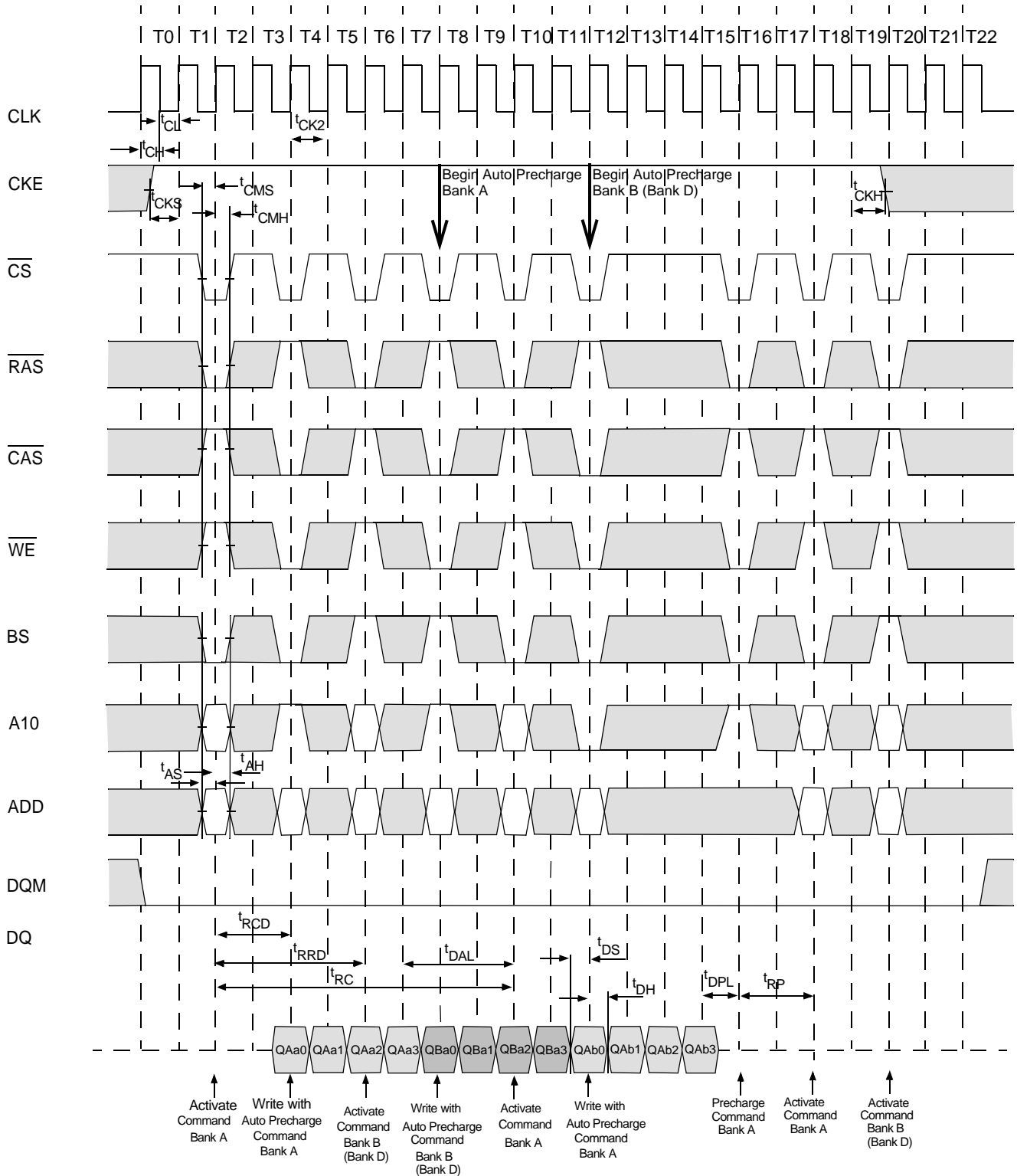
Timing Diagram

Mode Register Set



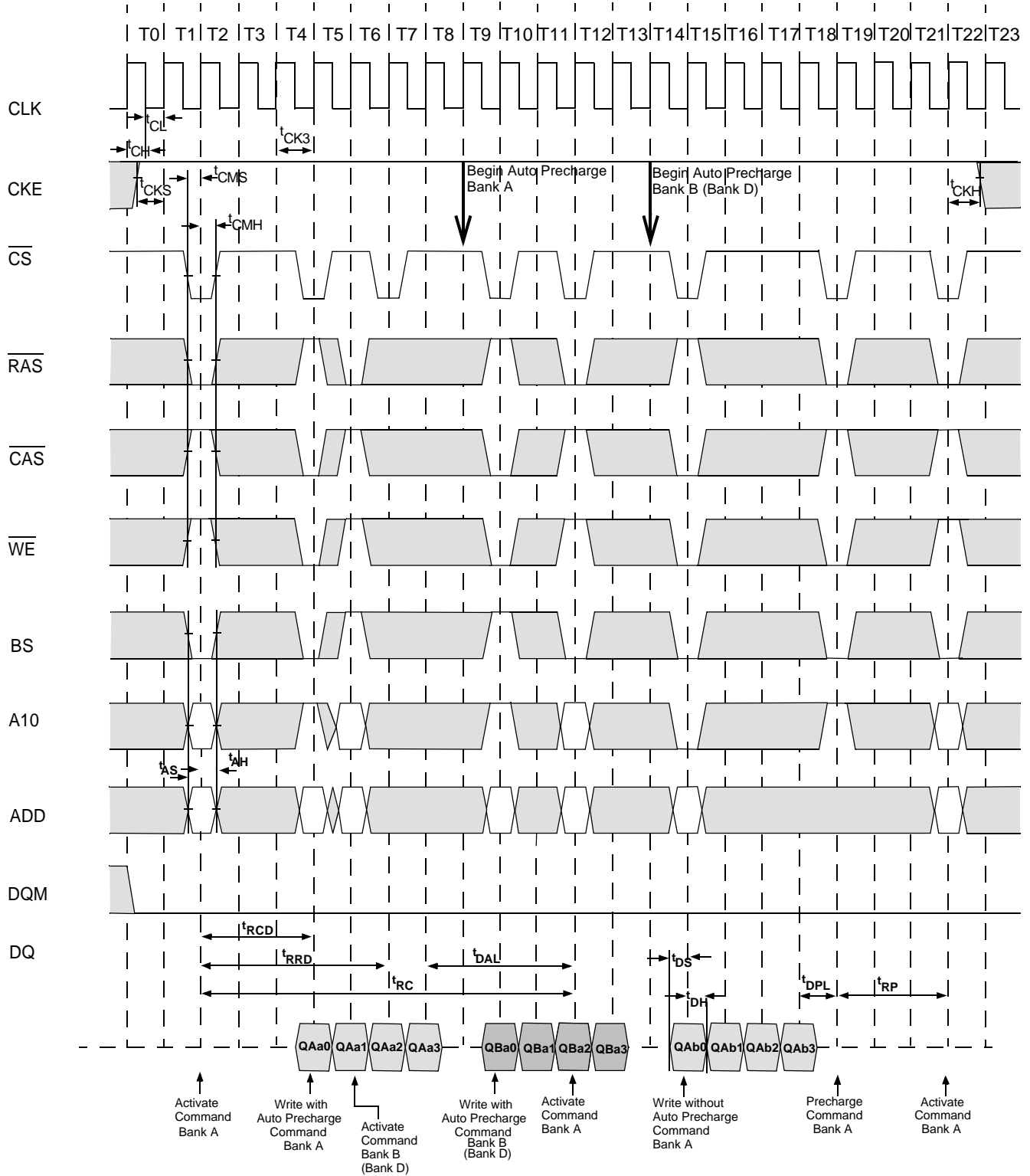
AC Parameters for Write Timing (1 of 2)

Burst Length = 4, CAS Latency = 2



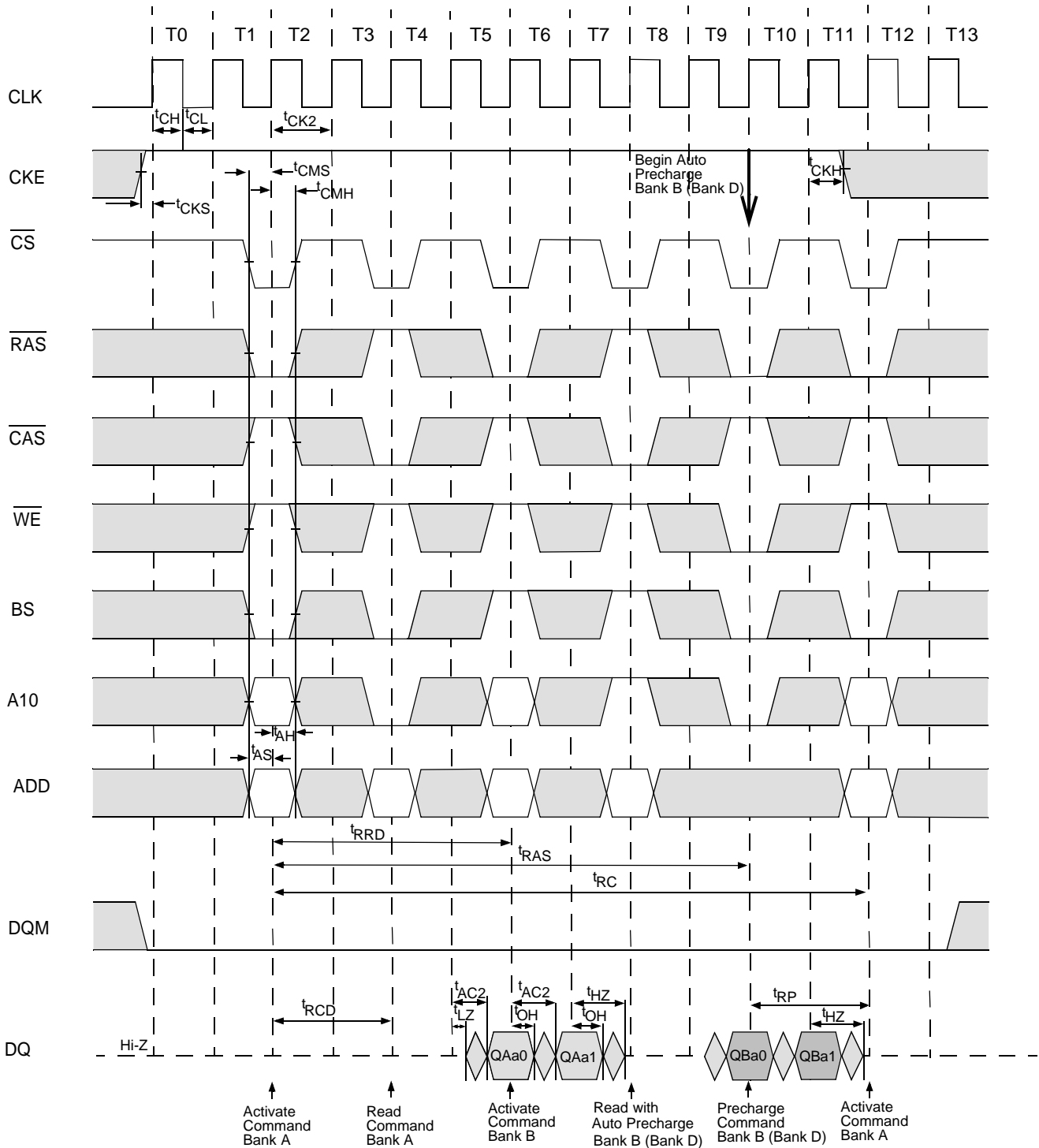
AC Parameters for Write Timing (2 of 2)

Burst Length = 4, CAS Latency = 3



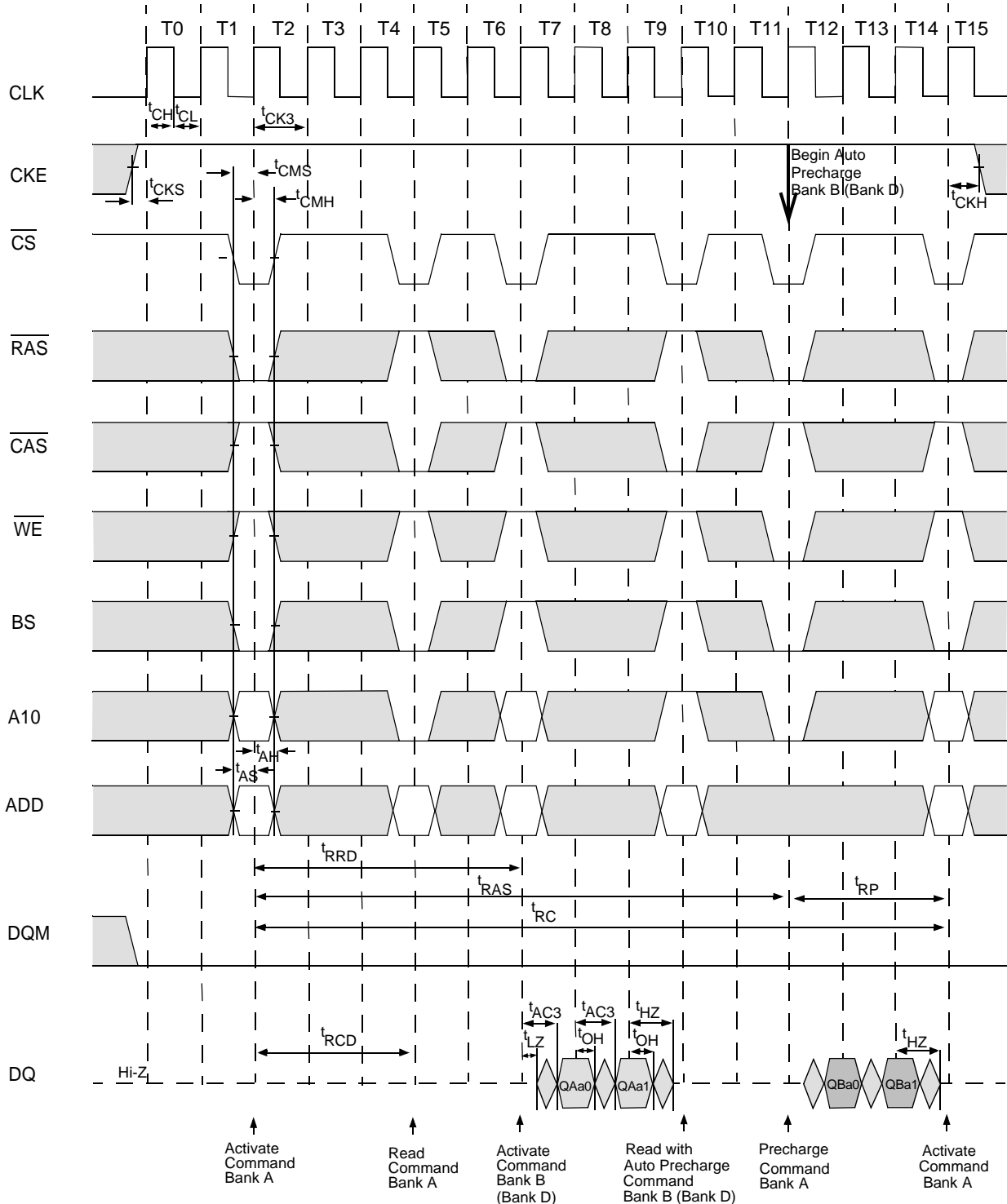
AC Parameters for Read Timing (1 of 2)

Burst Length = 2, $\overline{\text{CAS}}$ Latency = 2

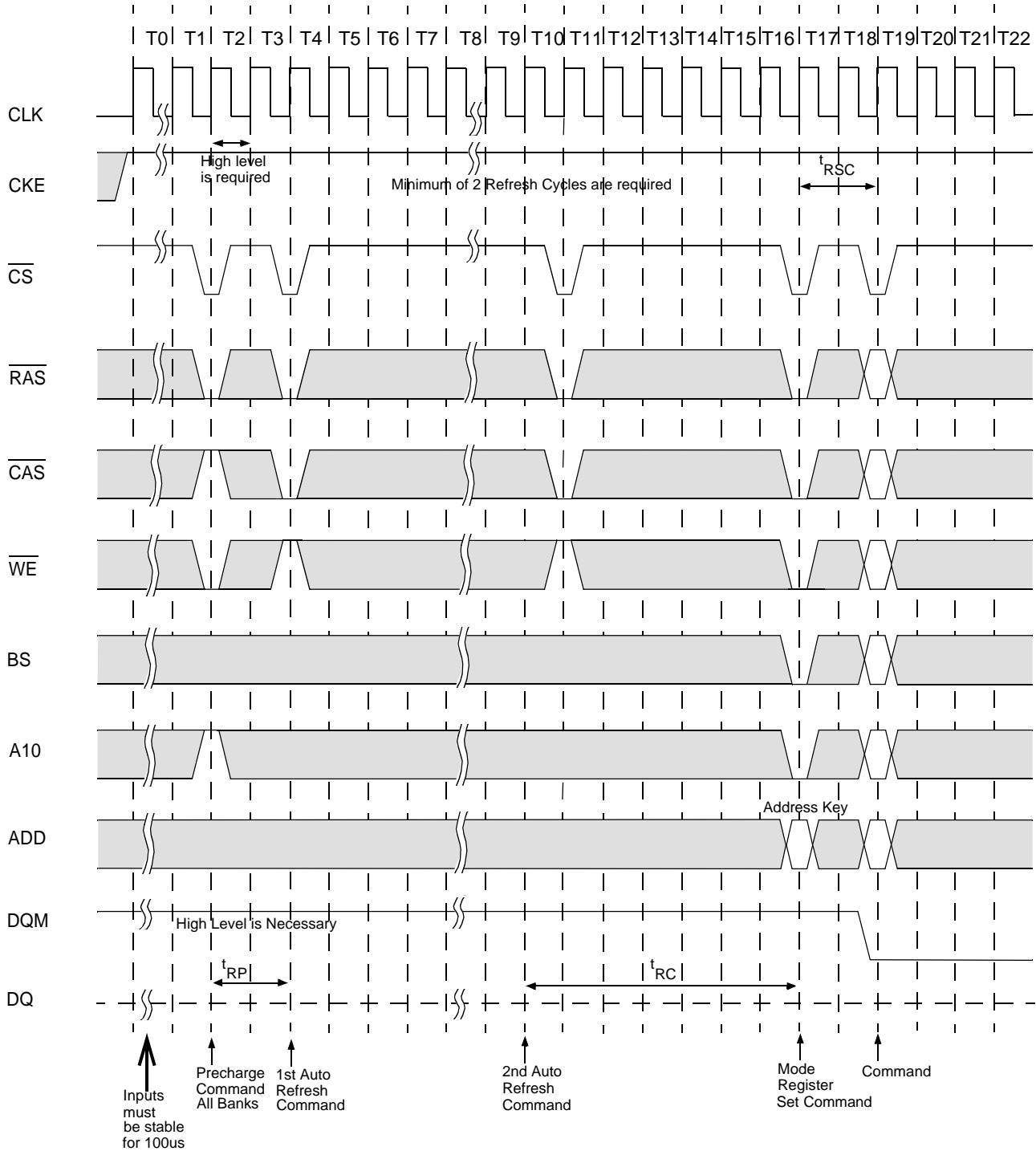


AC Parameters for Read Timing (2 of 2)

Burst Length = 2, CAS Latency = 3

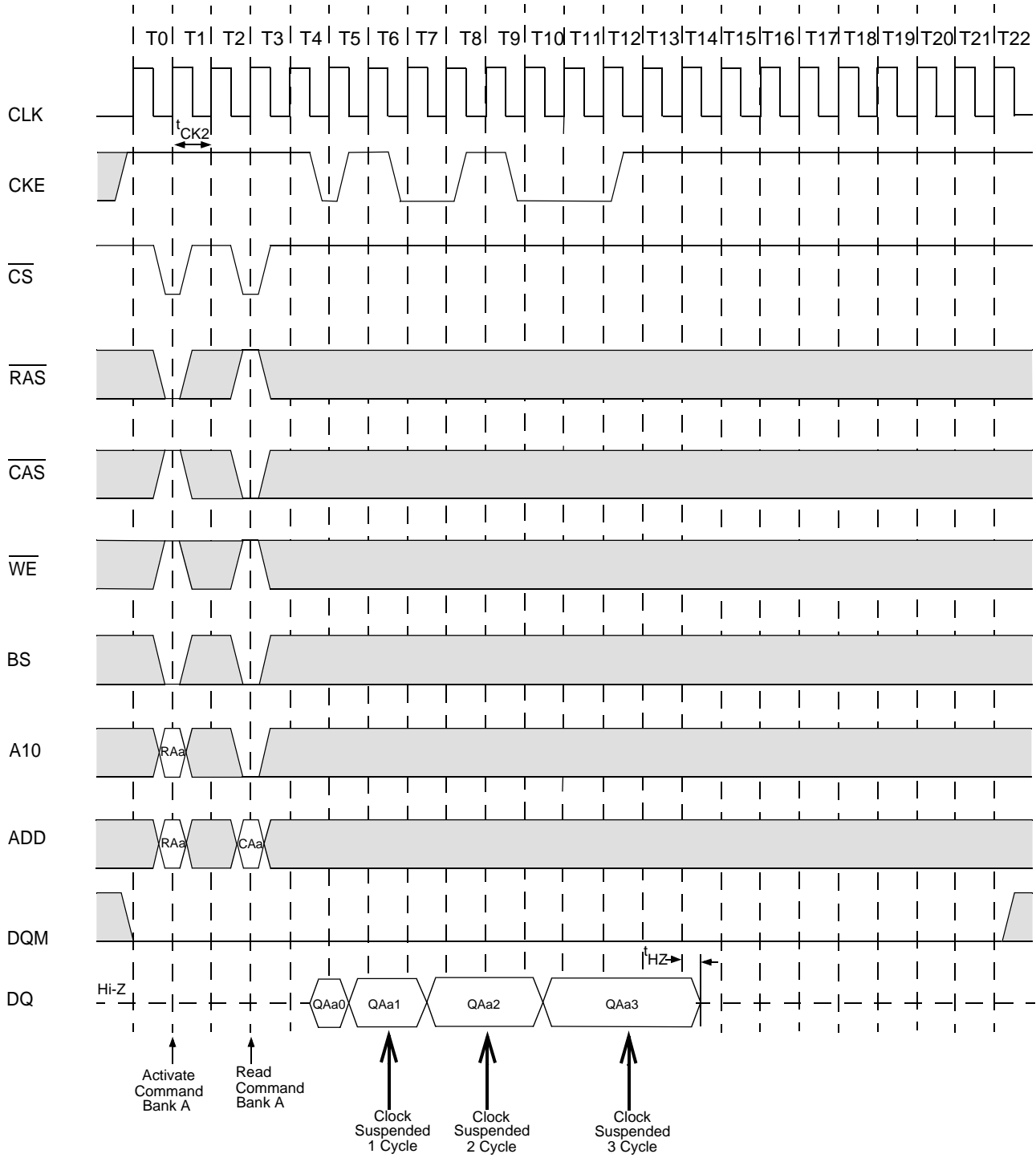


Power on Sequence and Auto Refresh (CBR)



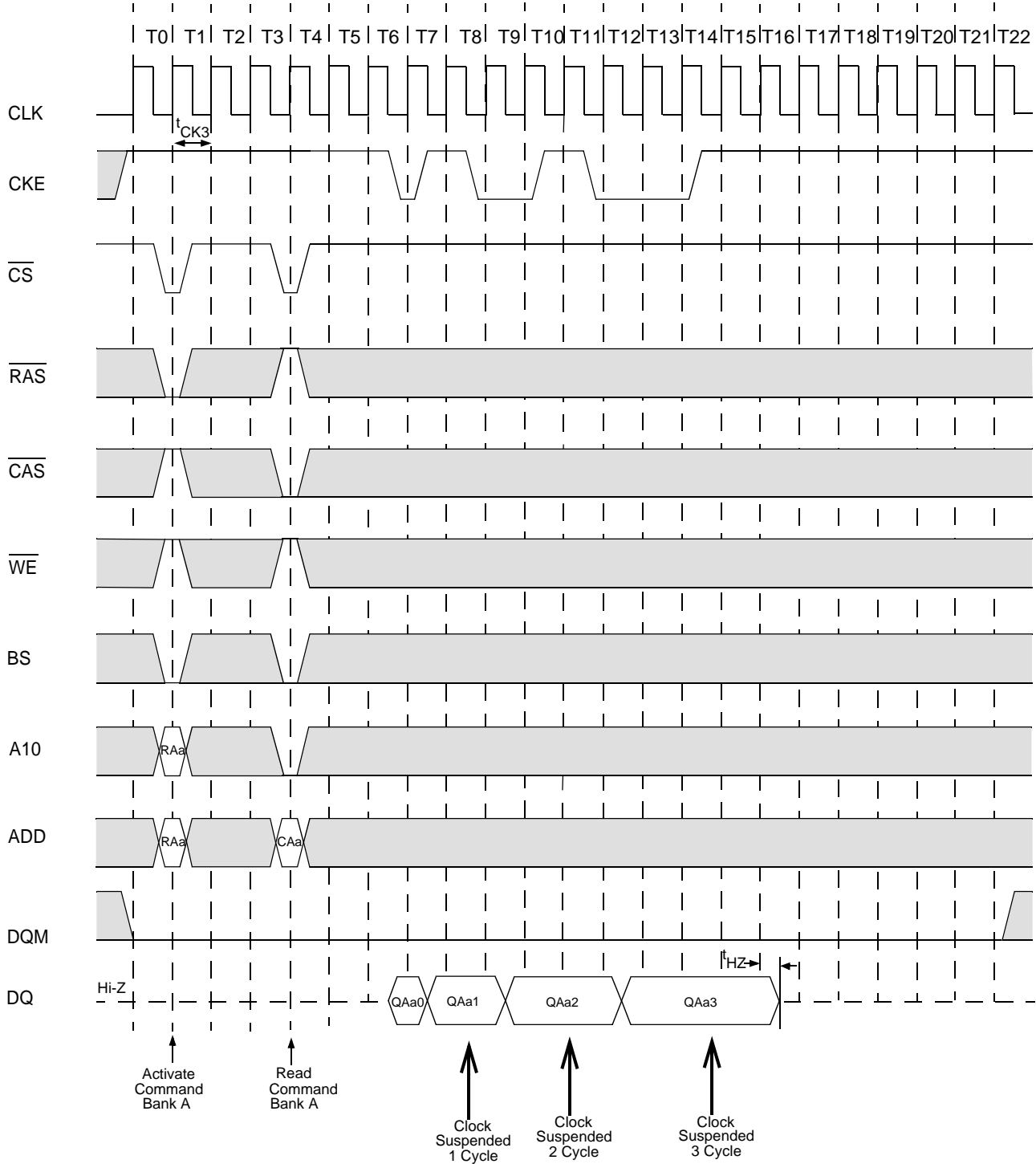
Clock Suspension During Burst Read (Using CKE) (1 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2



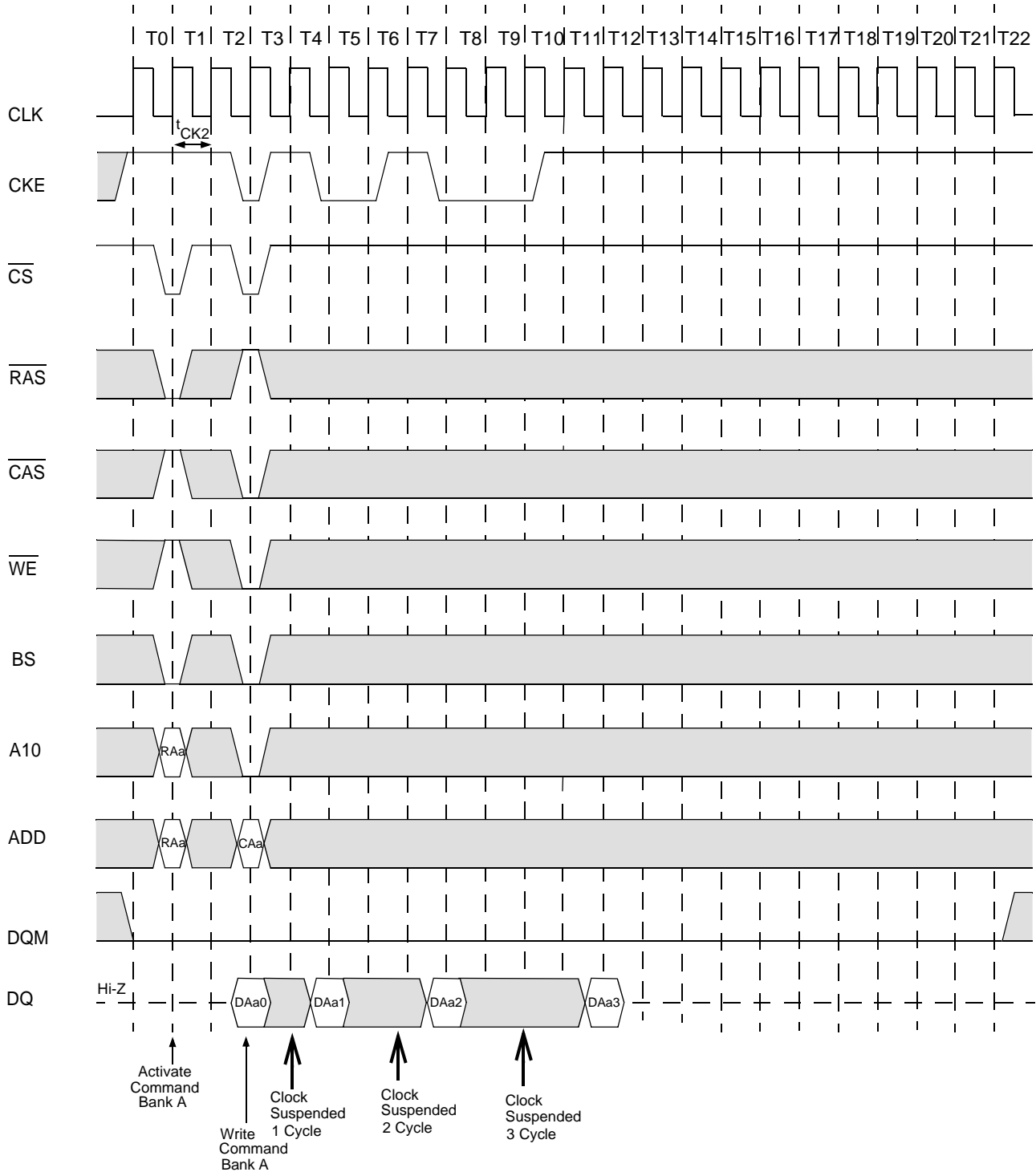
Clock Suspension During Burst Read (Using CKE) (2 of 2)

Burst Length = 4, CAS Latency = 3



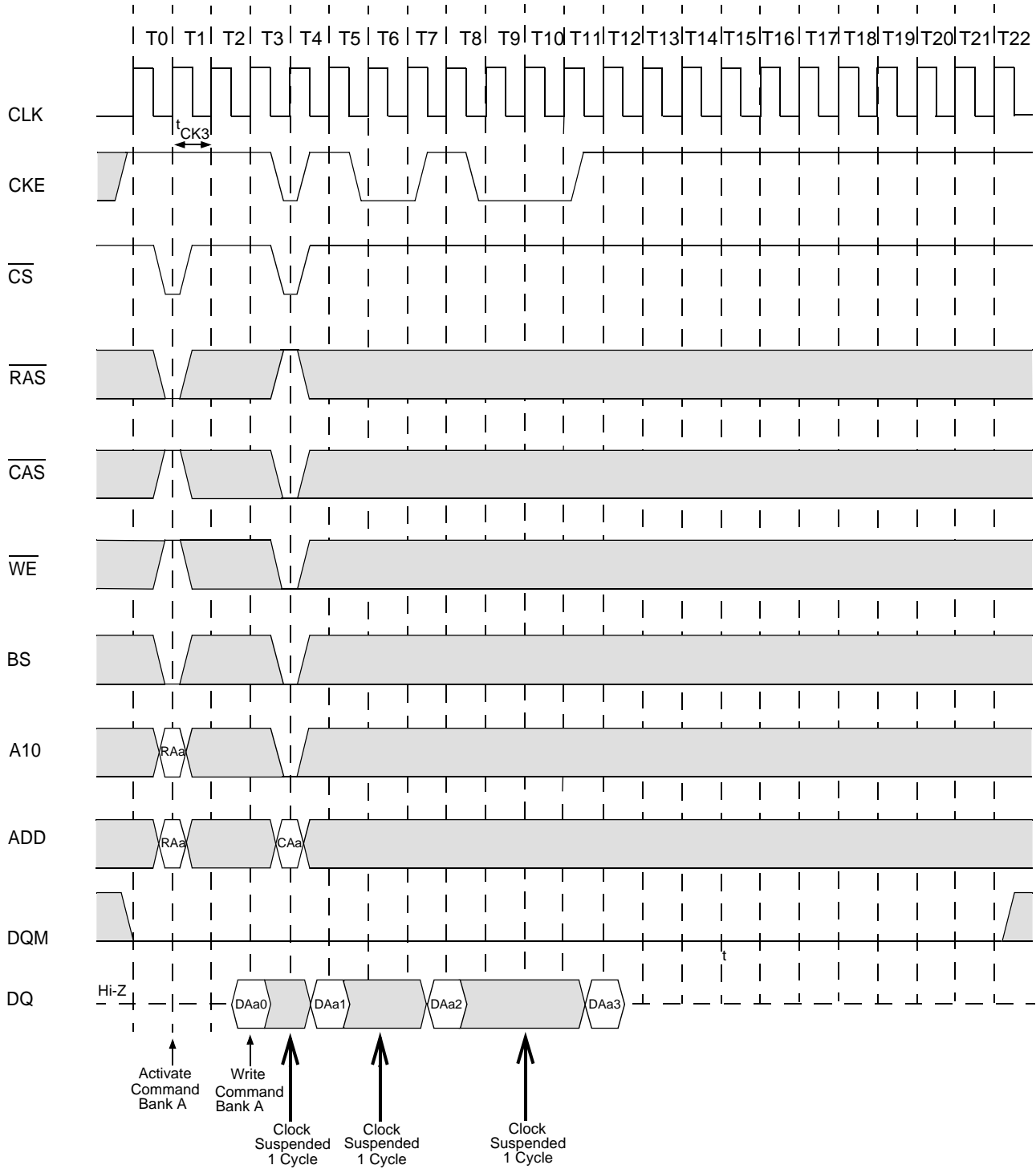
Clock Suspension During burst Write (Using CKE) (1 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2



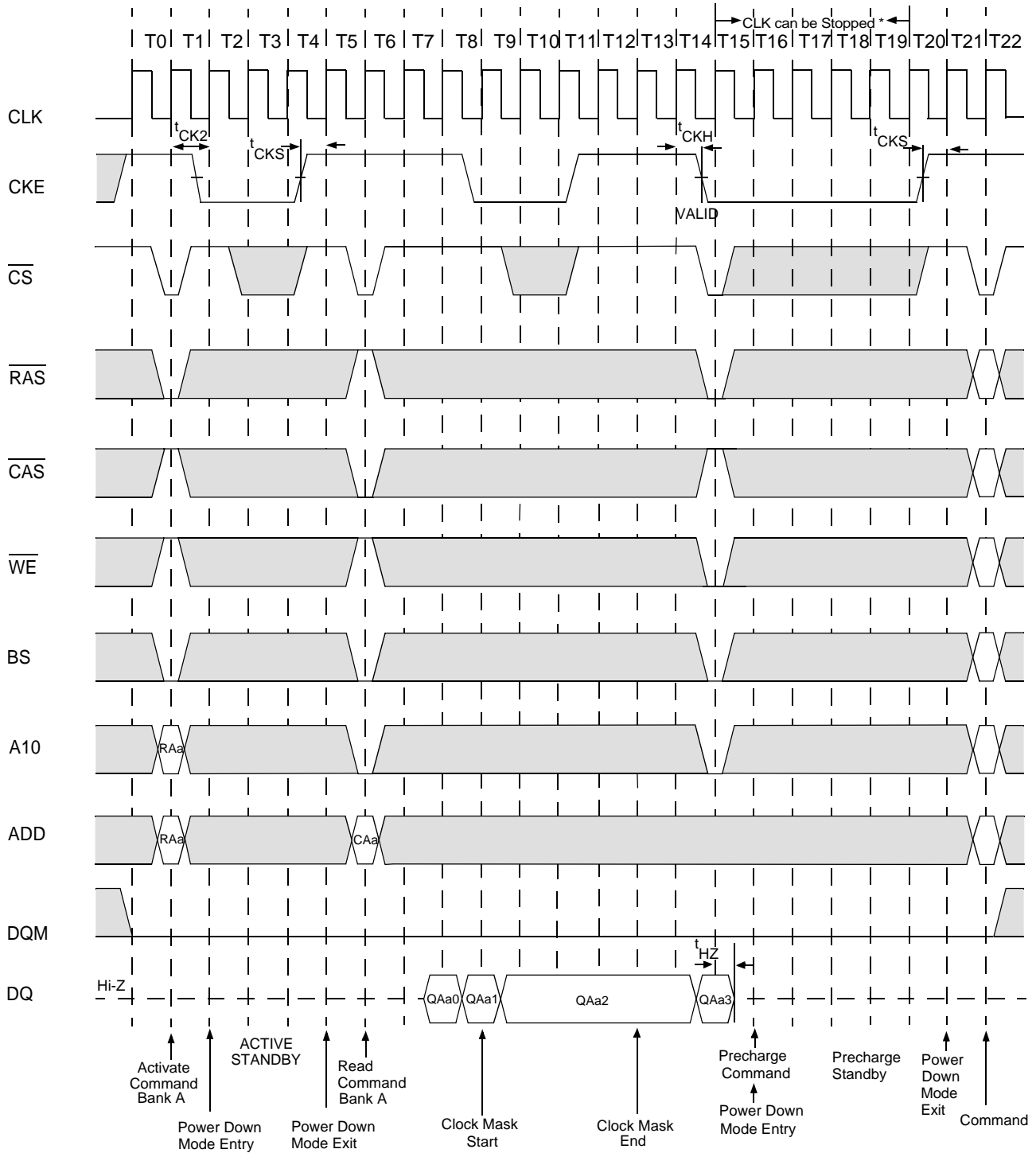
Clock suspension during Burst write (Using CKE) (2 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3



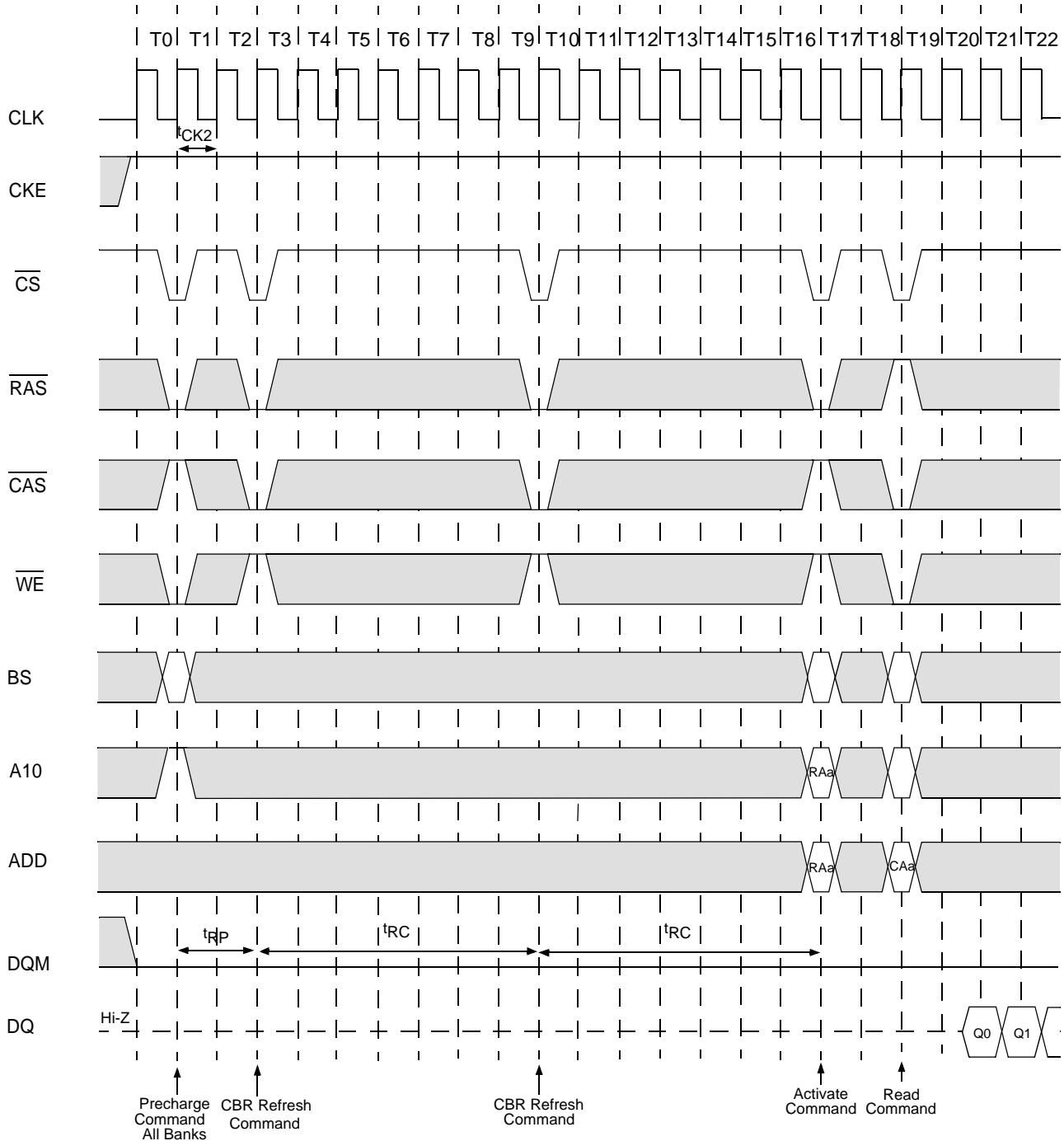
Power Down Mode and Clock Mask

Burst Length = 4, CAS Latency = 2

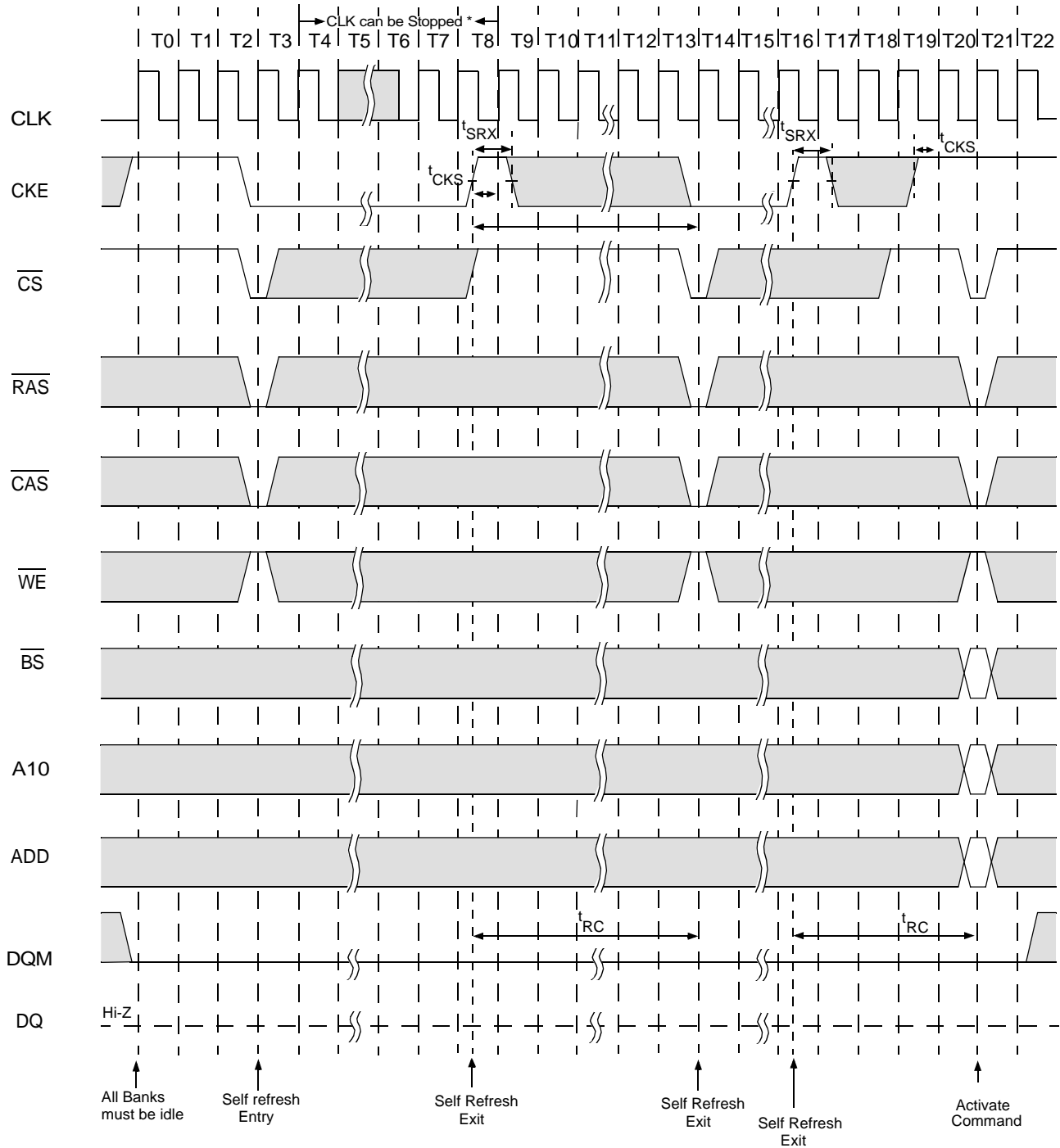


Auto Refresh (CBR)

Burst Length = 4, CAS Latency = 2

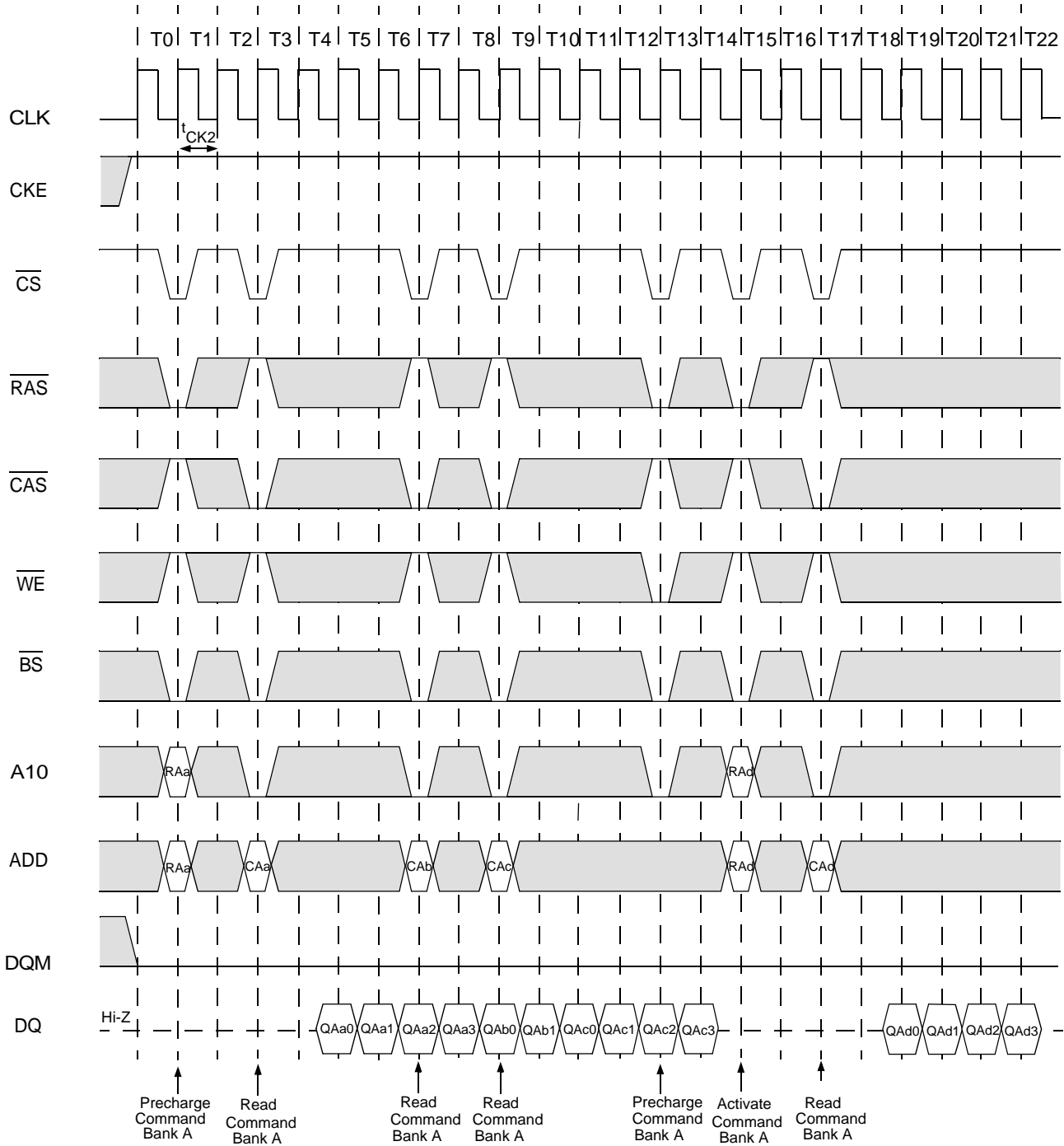


Self Refresh (Entry and Exit)



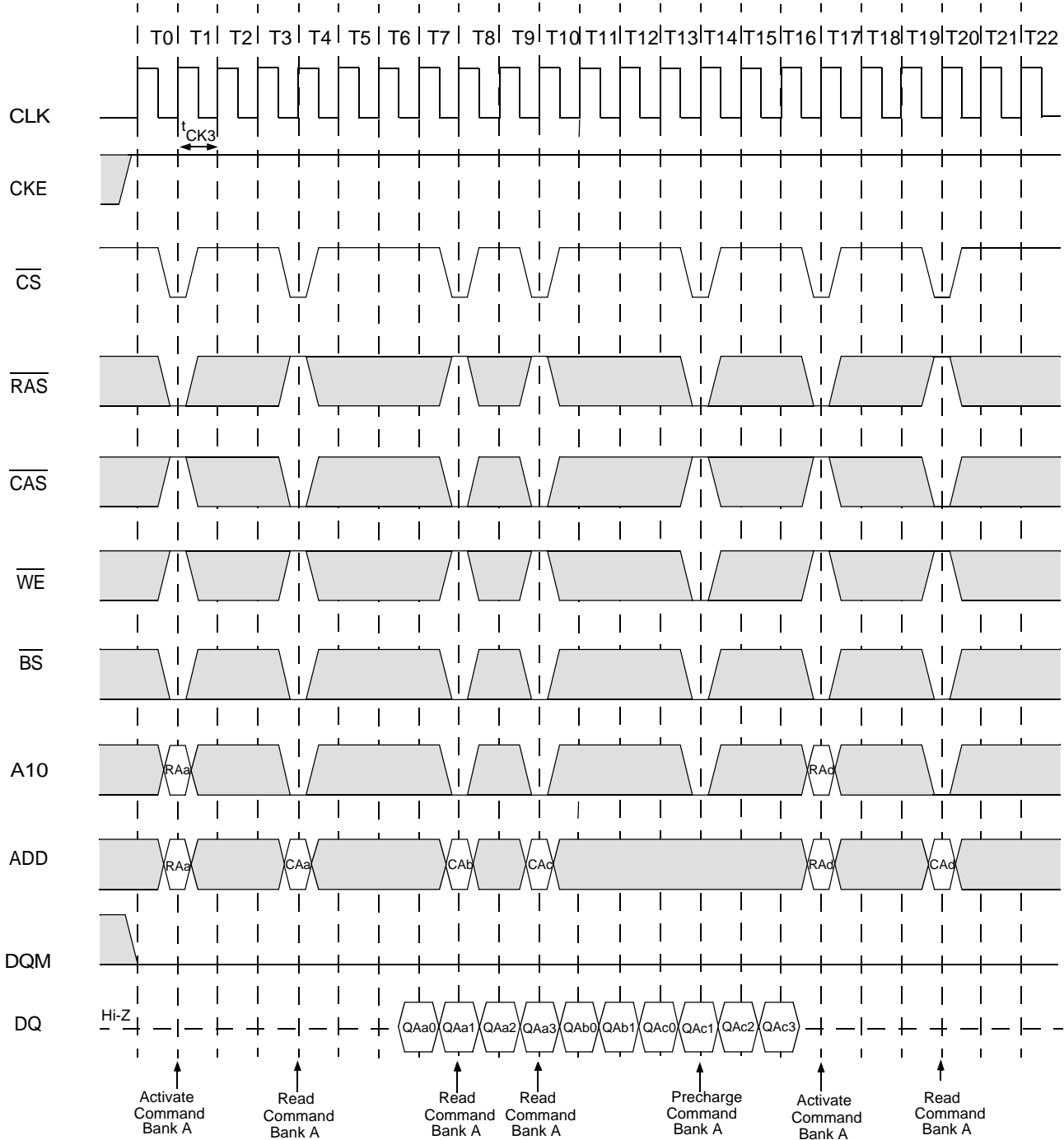
Random Column Read (Page Within same Bank)(1 of 2)

Burst Length = 4, CAS Latency = 2



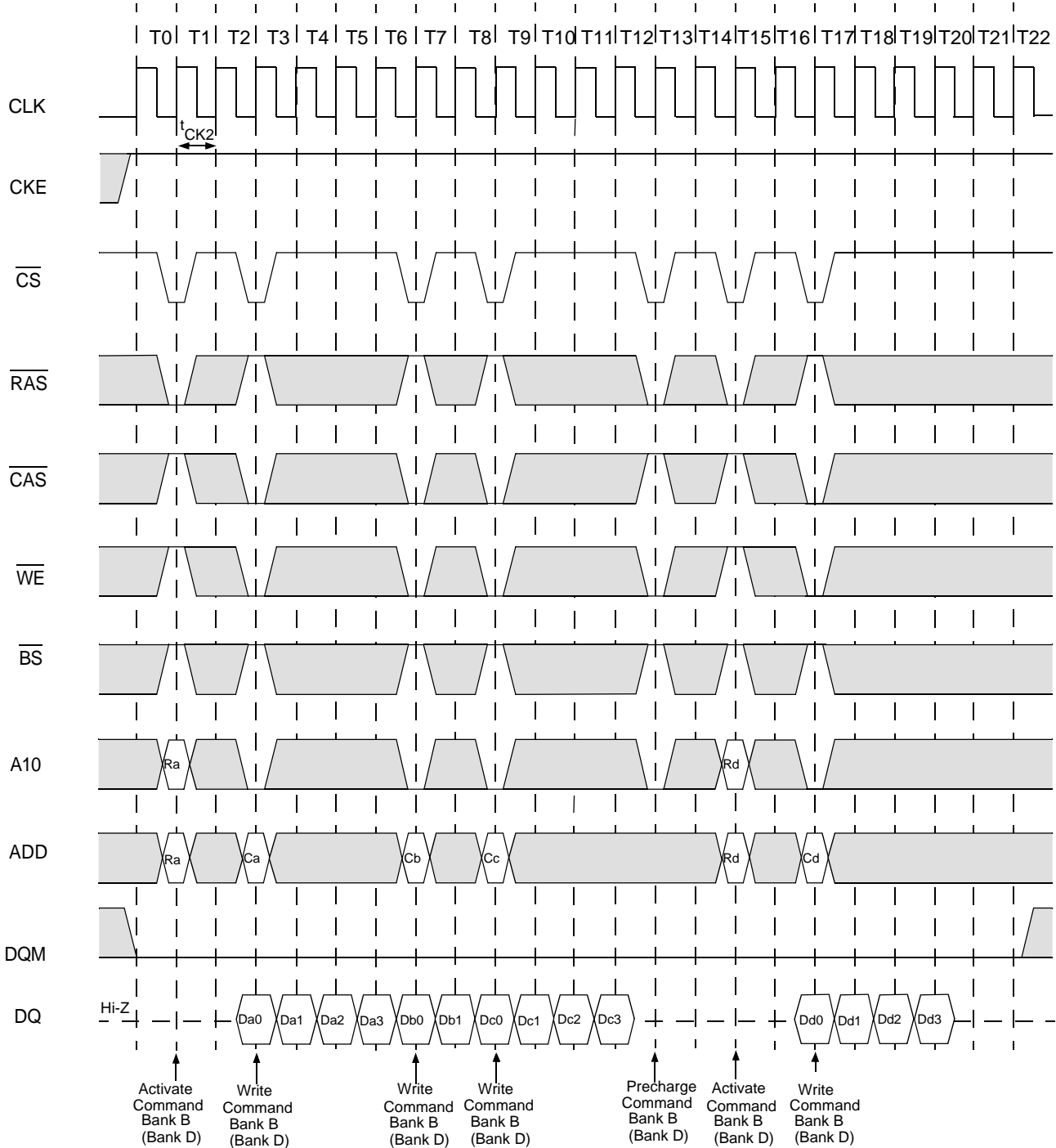
Random Column Read (Page Within same Bank)(2 of 2)

Burst Length = 4, CAS Latency = 3



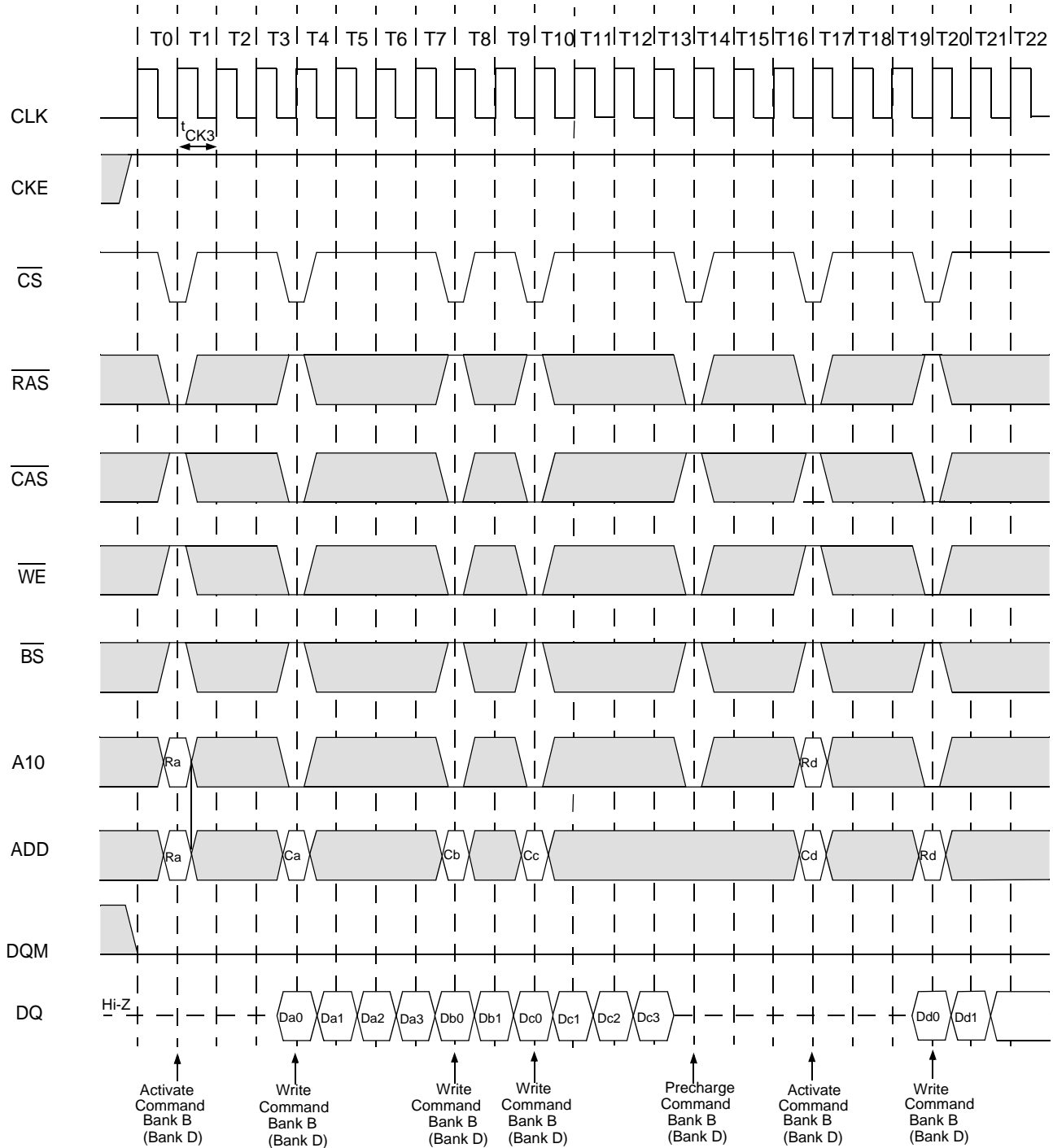
Random Column Write (Page Within same Bank) (1 of 2)

Burst Length = 4, CAS Latency = 2



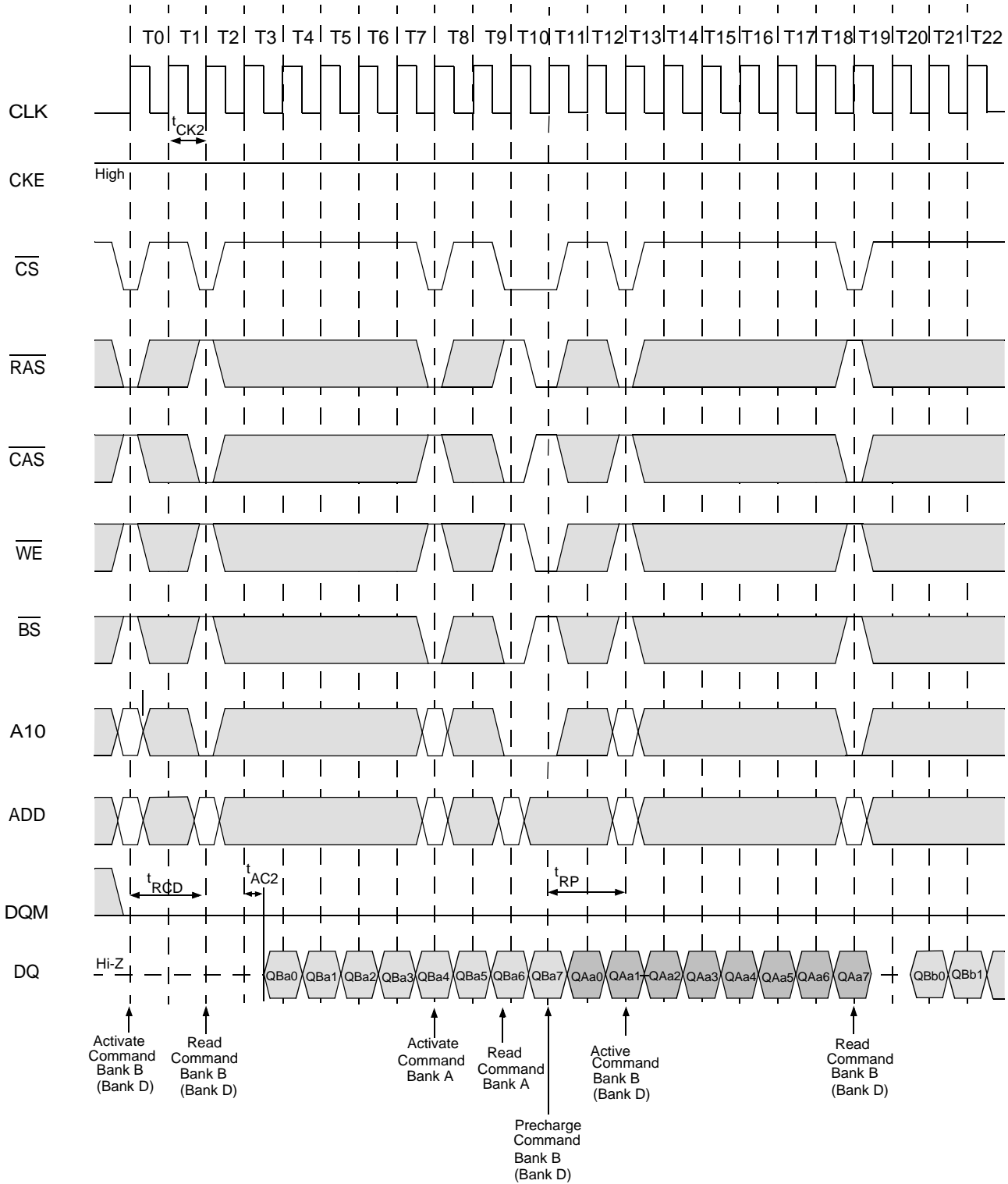
Random Column Write (Page Within same Bank) (2 of 2)

Burst Length = 4, CAS Latency = 3



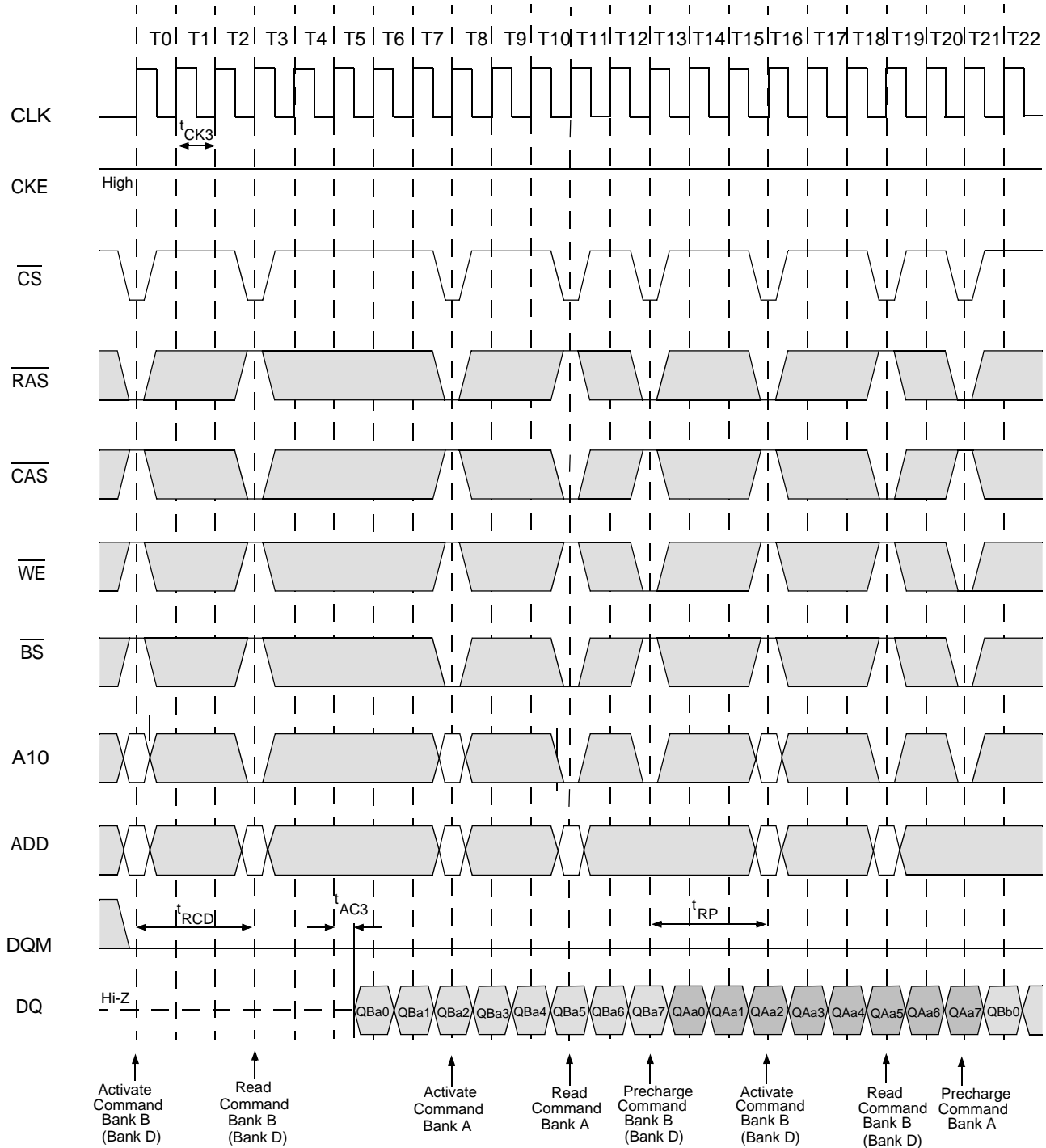
Random Row Read (Interleaving Banks) (1 of 2)

Burst Length = 8, CAS Latency = 2



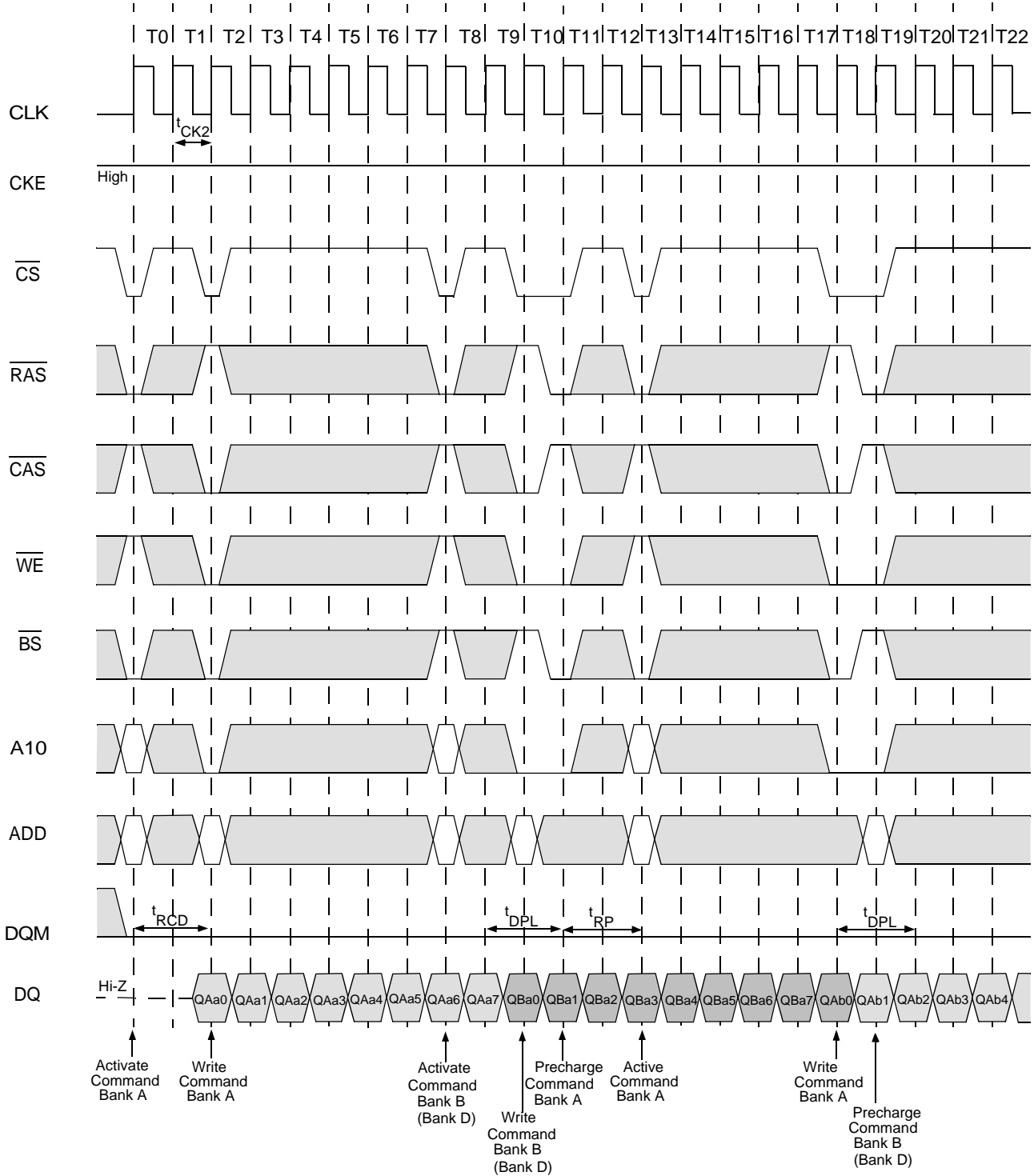
Random Row Read (Interleaving Banks) (2 of 2)

Burst Length = 8, CAS Latency = 3



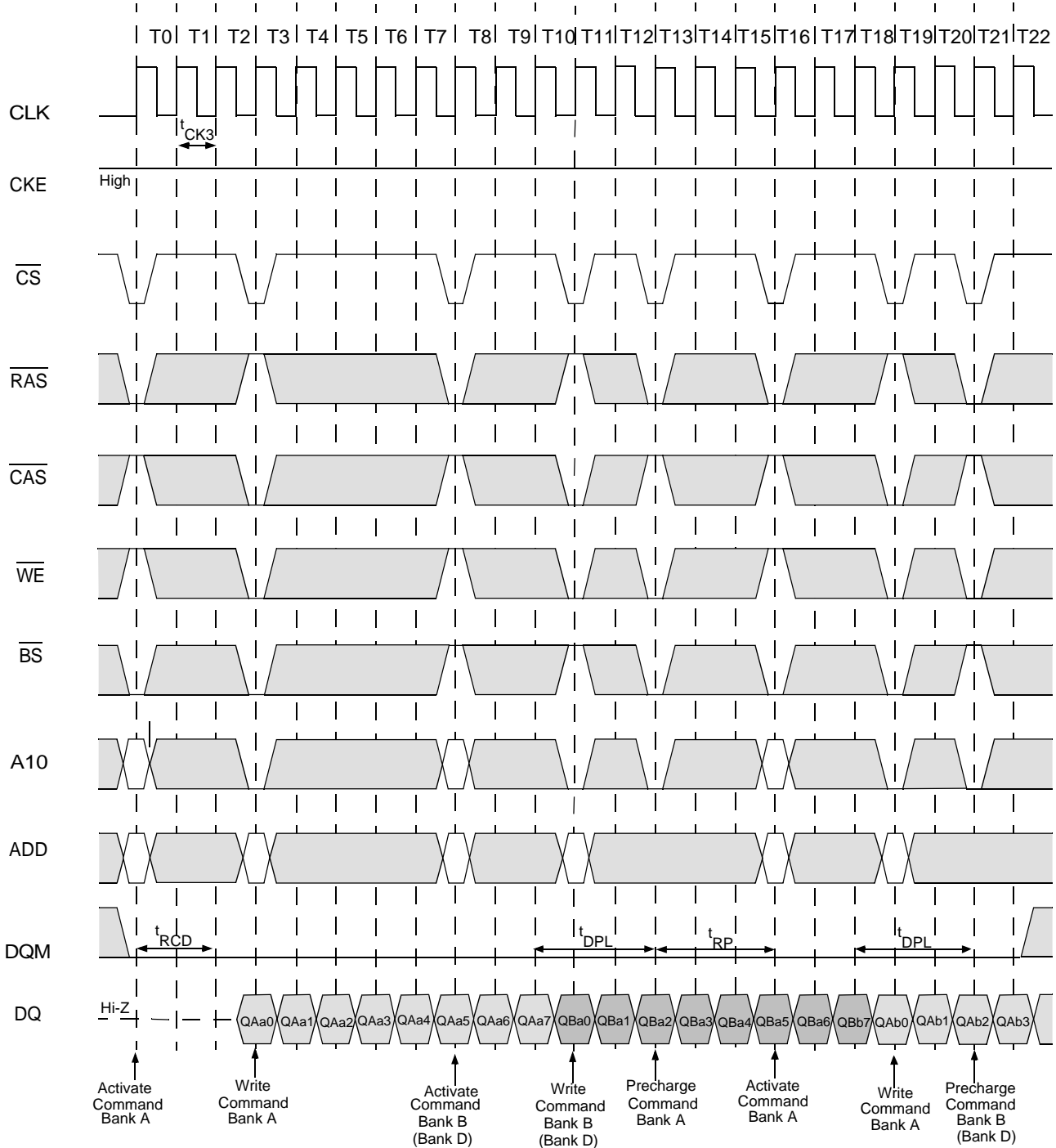
Random Row Write (Interleaving Banks) (1 of 2)

Burst Length = 8, CAS Latency = 2



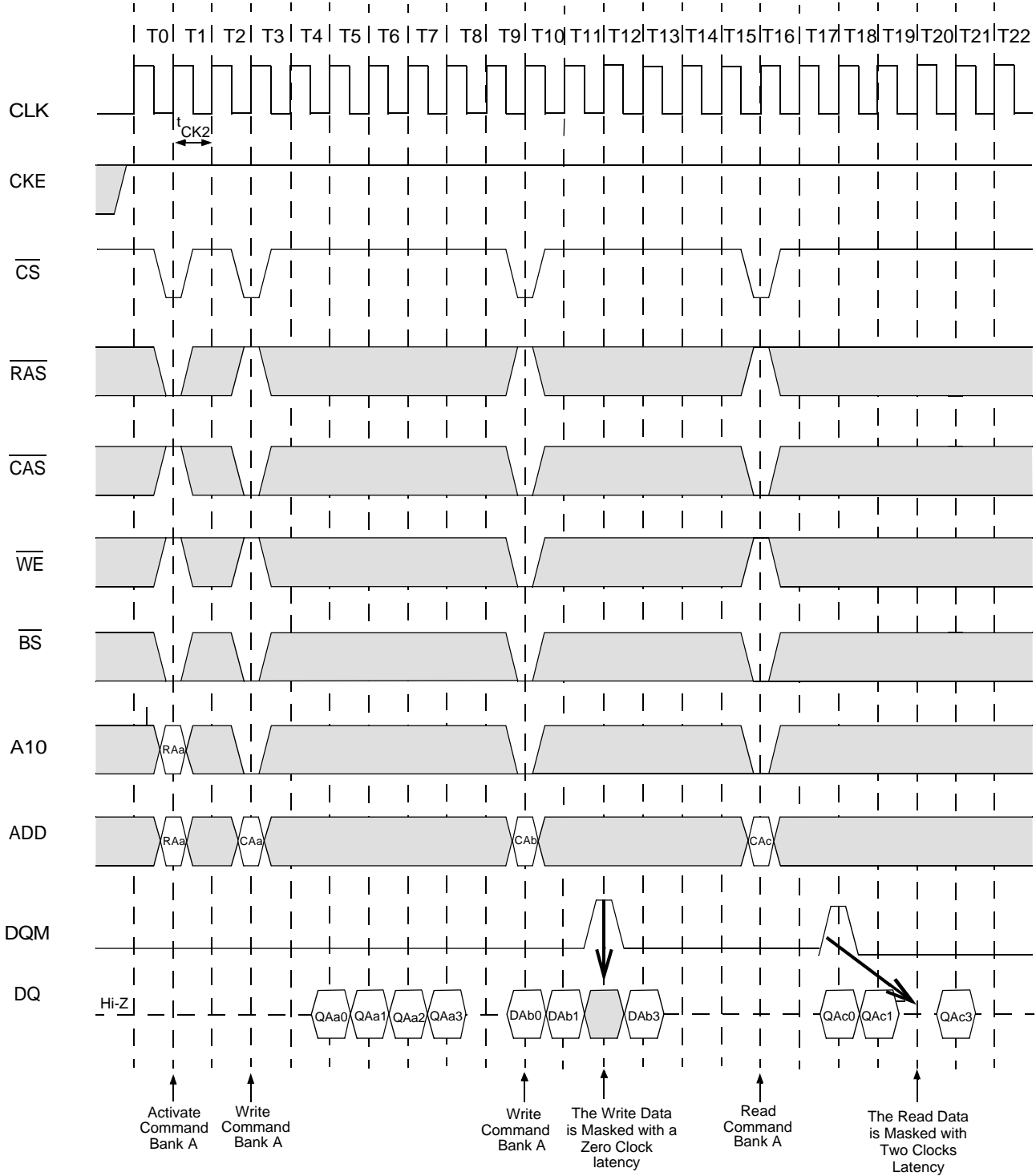
Random Row Write (Interleaving Banks) (2 of 2)

Burst Length = 8, CAS Latency = 3



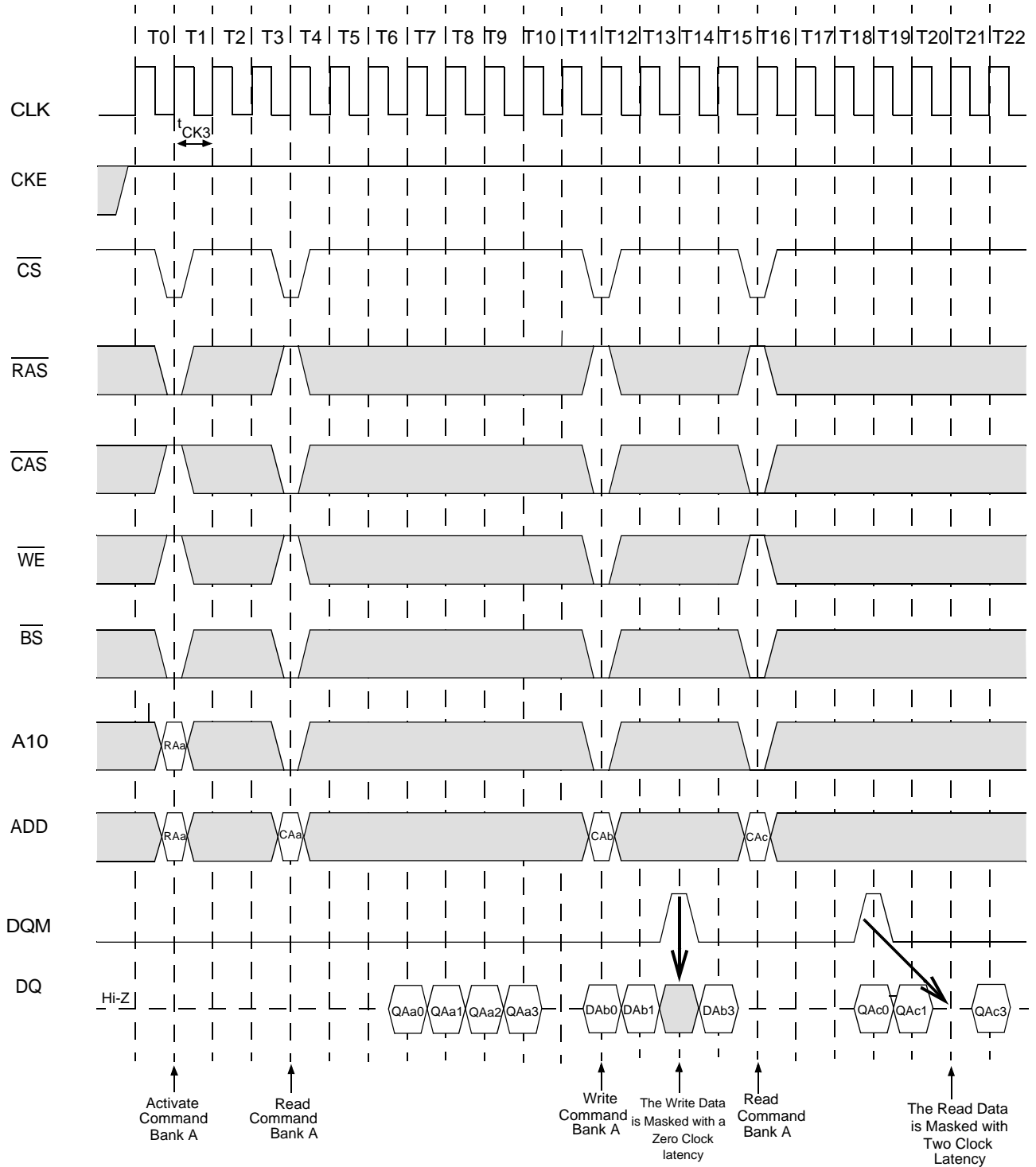
Read and Write Cycle (1 of 2)

Burst Length = 4, CAS Latency = 2



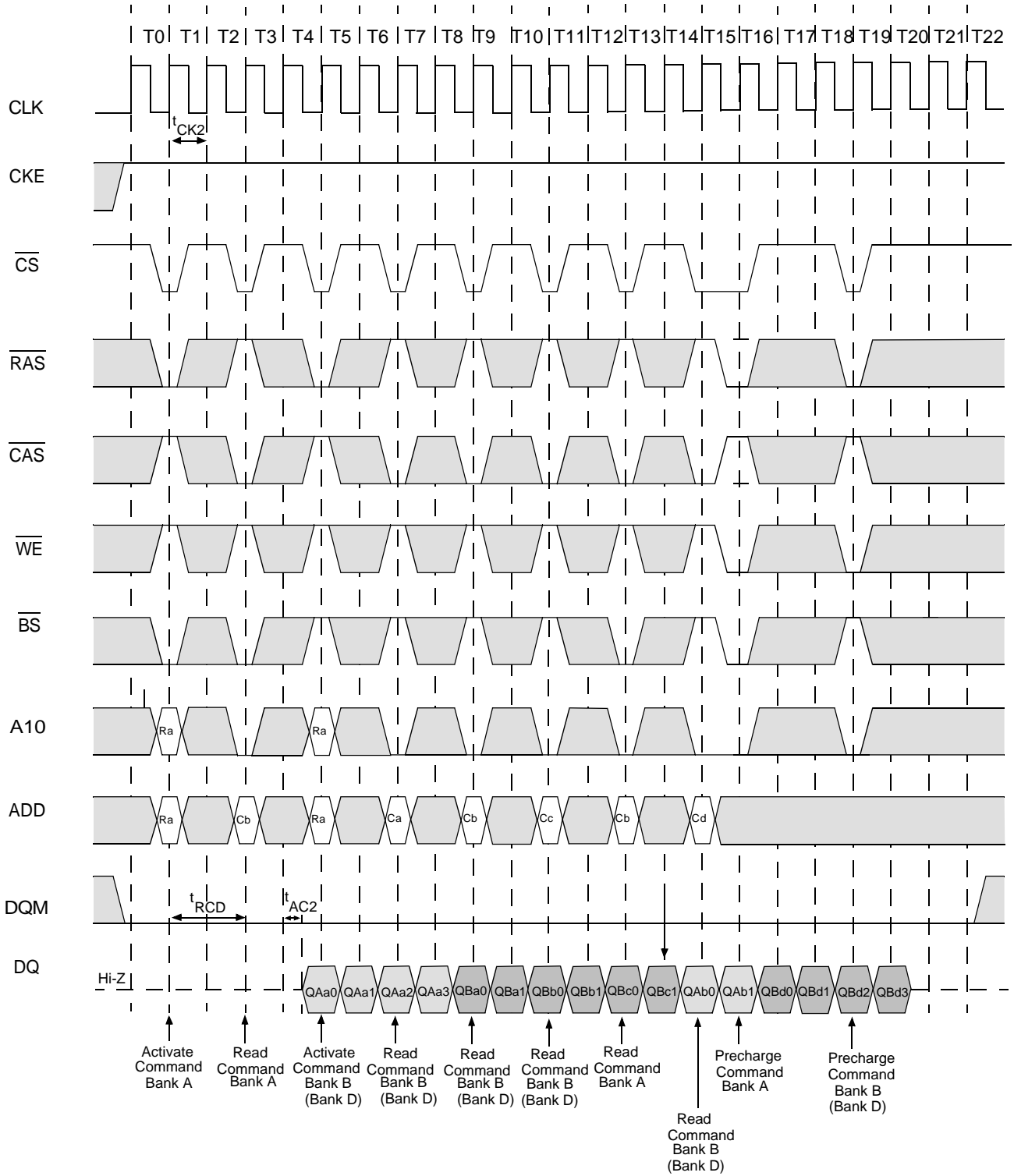
Read and Write Cycle (2 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3



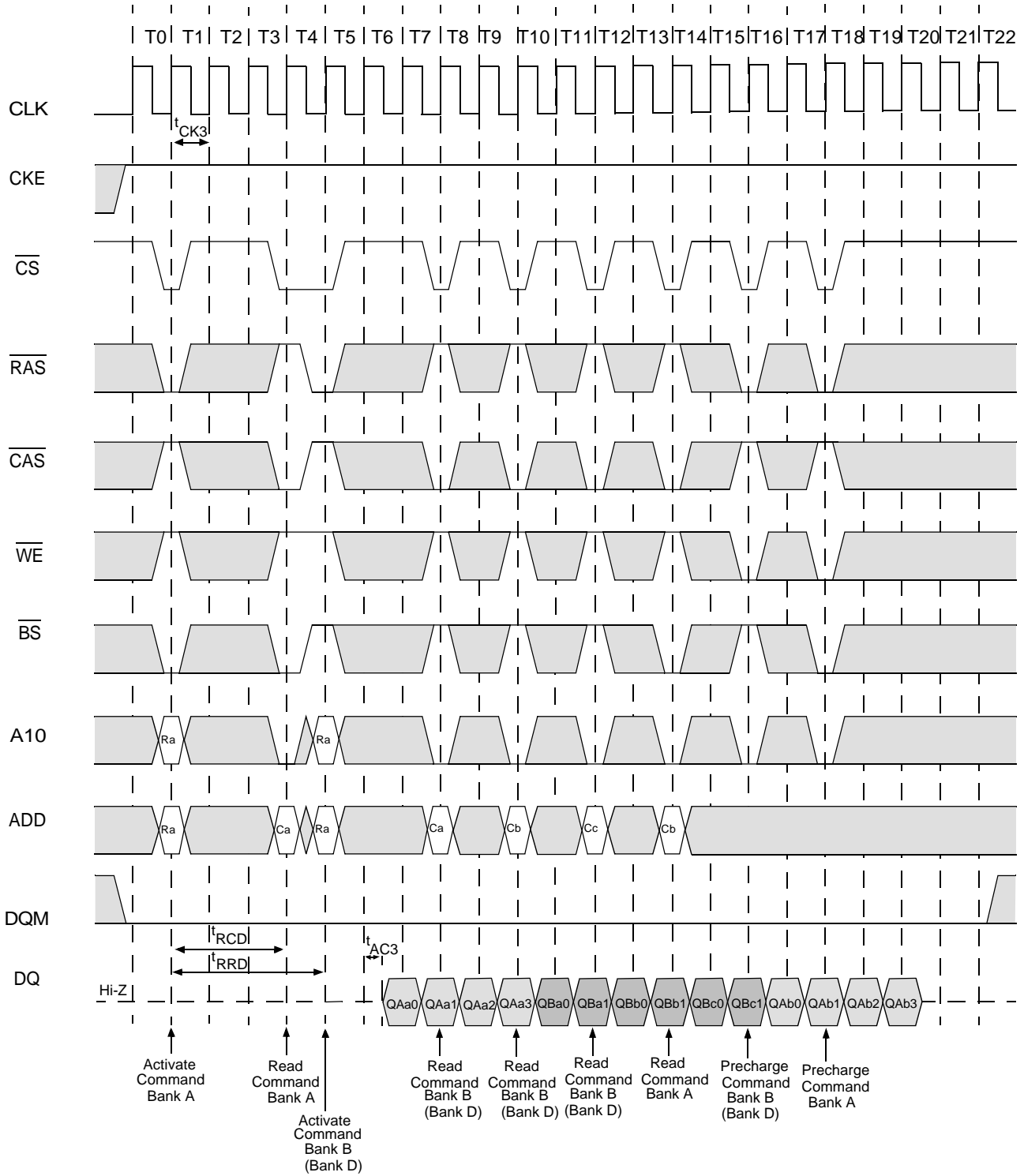
Interleaved Column Read Cycle (1 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2



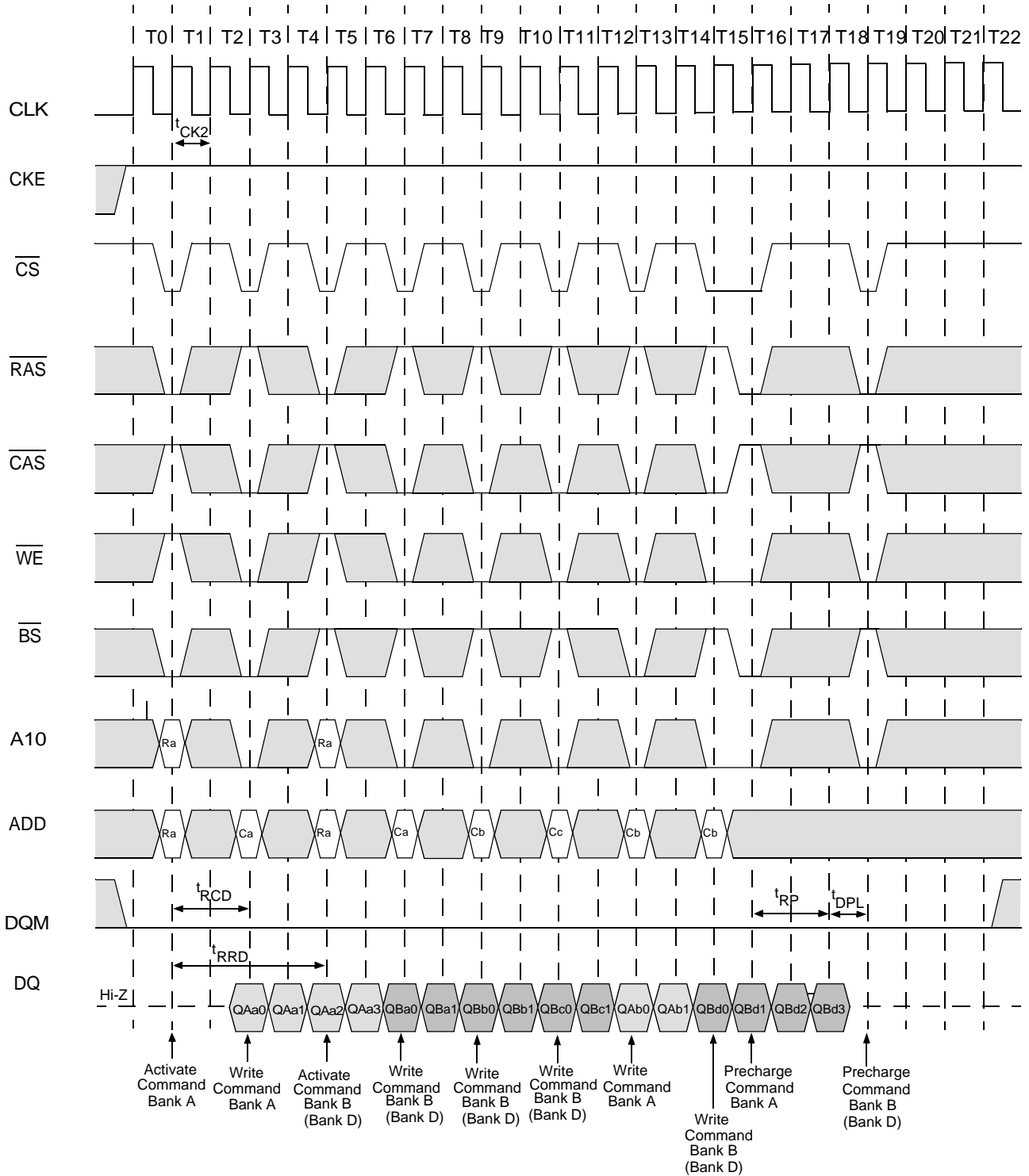
Interleaved Column Read Cycle (2 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3



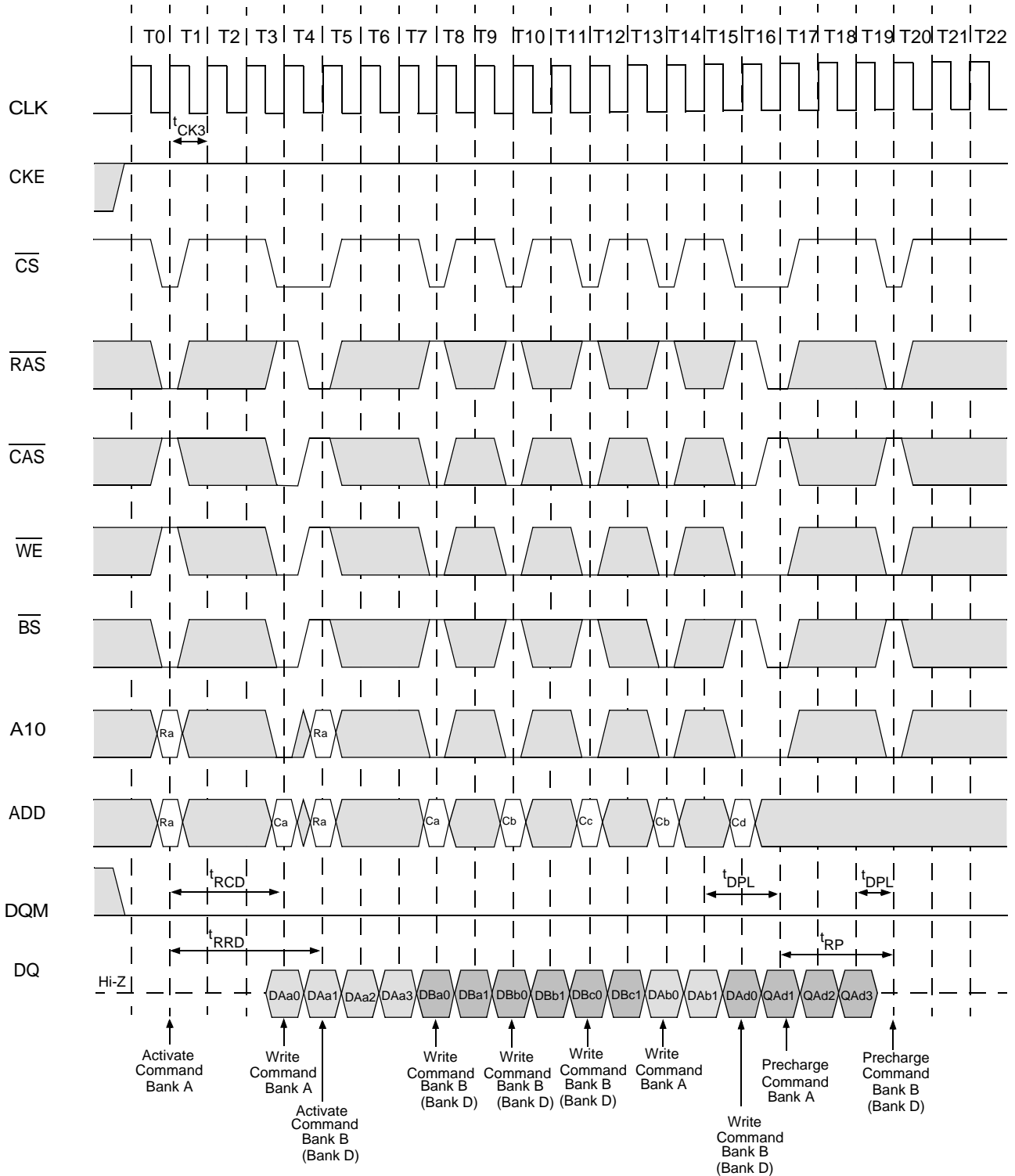
Interleaved Column Write Cycle (1 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2



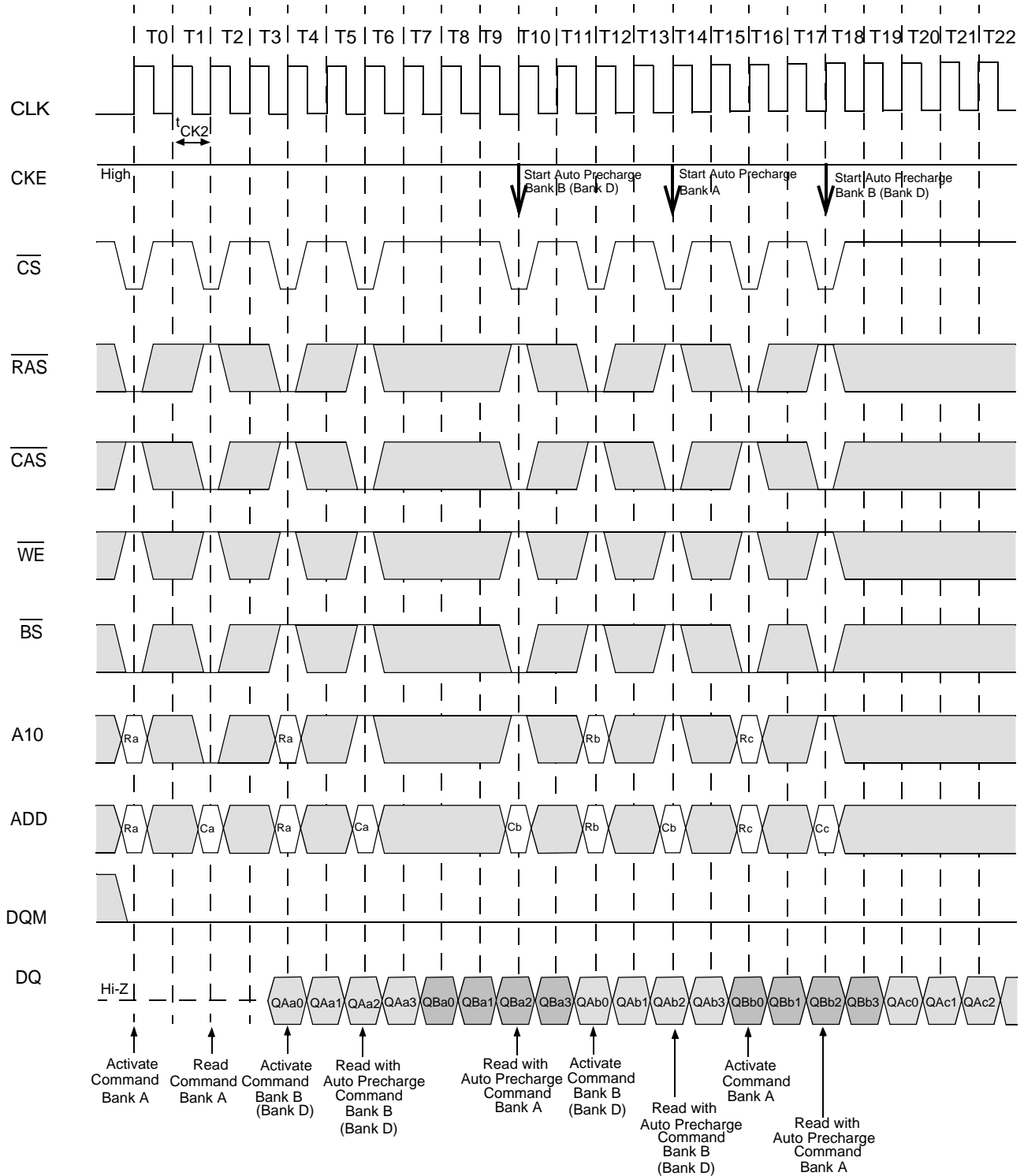
Interleaved Column Write Cycle (2 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3



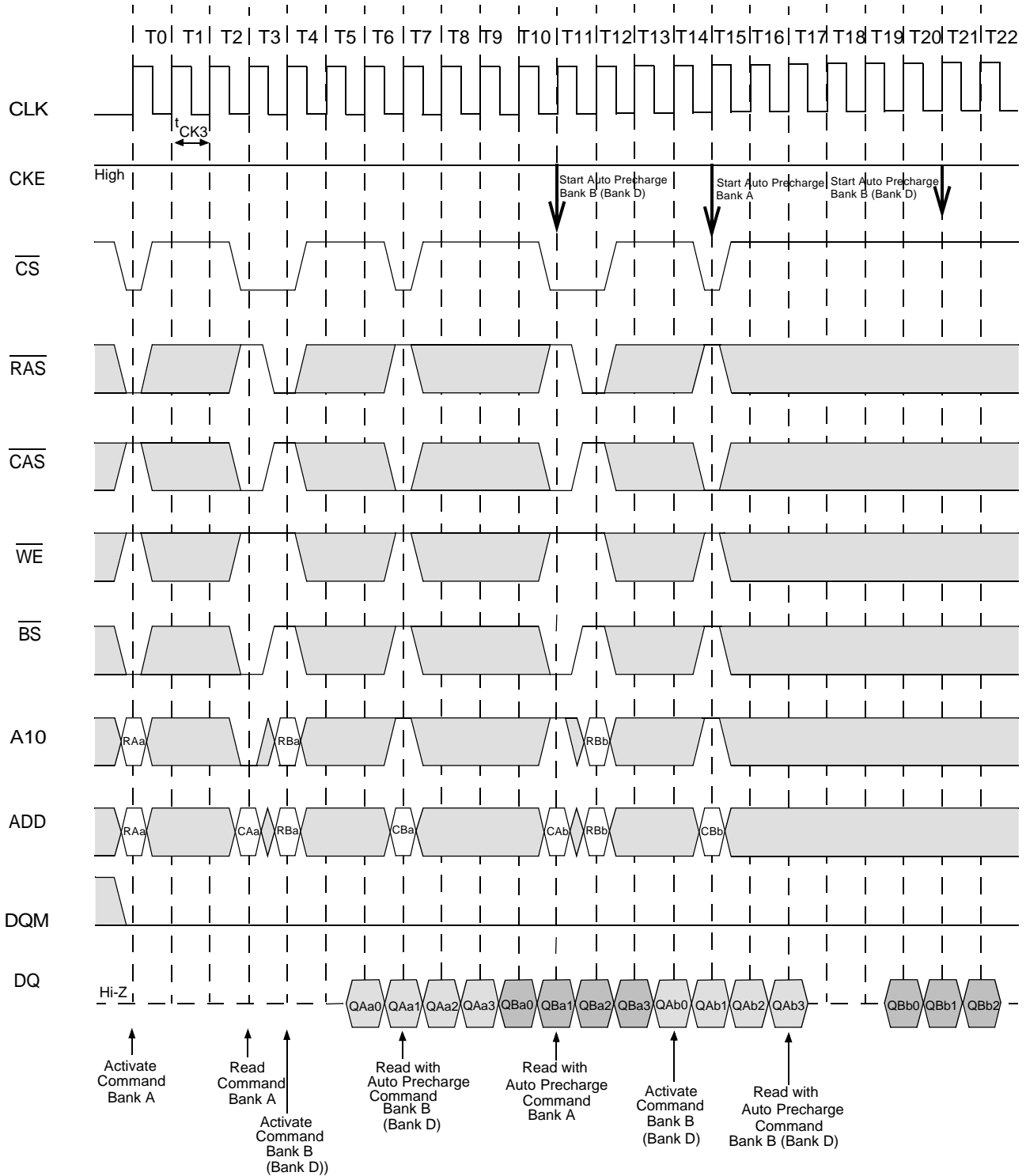
Auto Precharge after Read Burst (1 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2



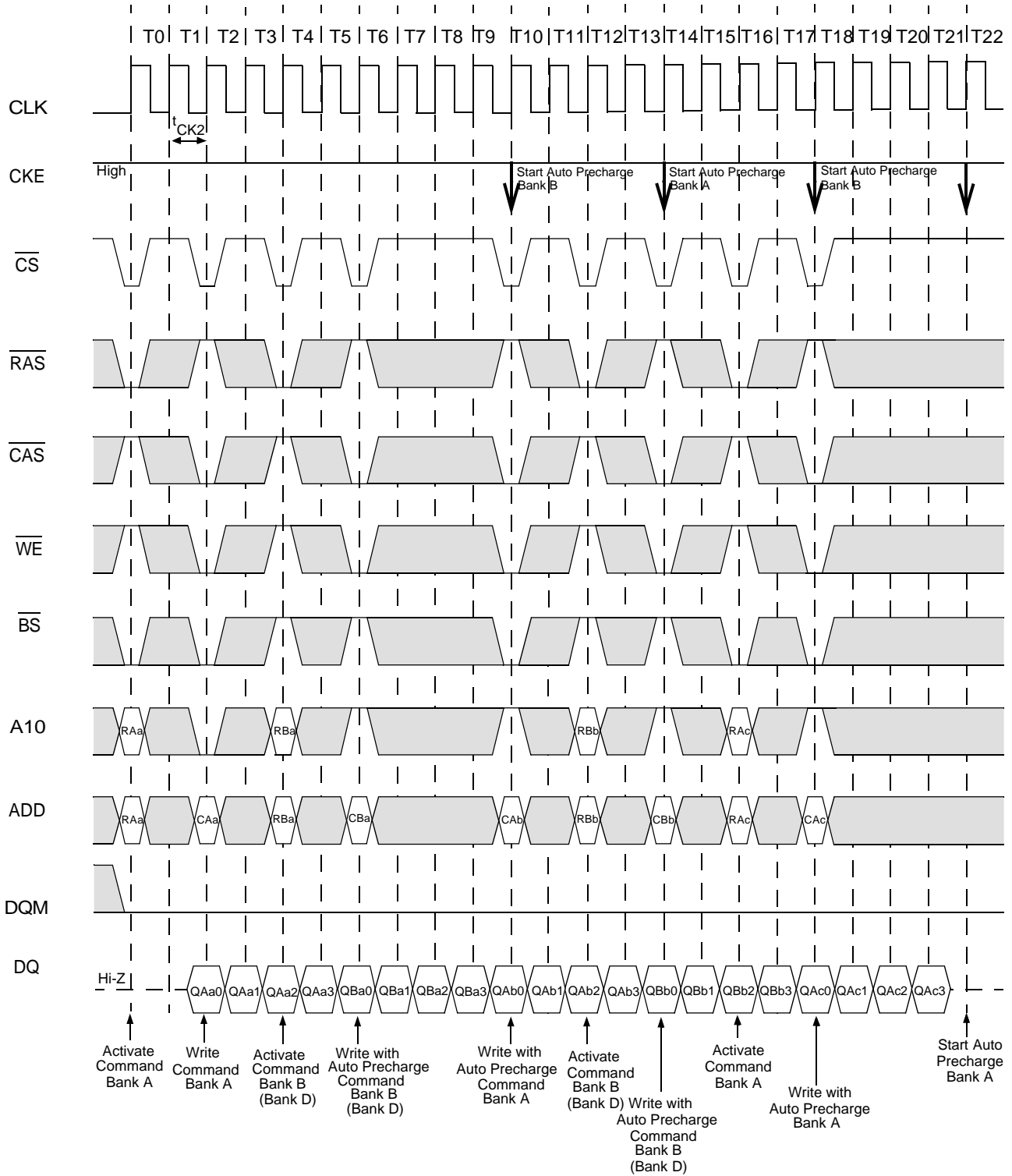
Auto Precharge after Read Burst (2 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3



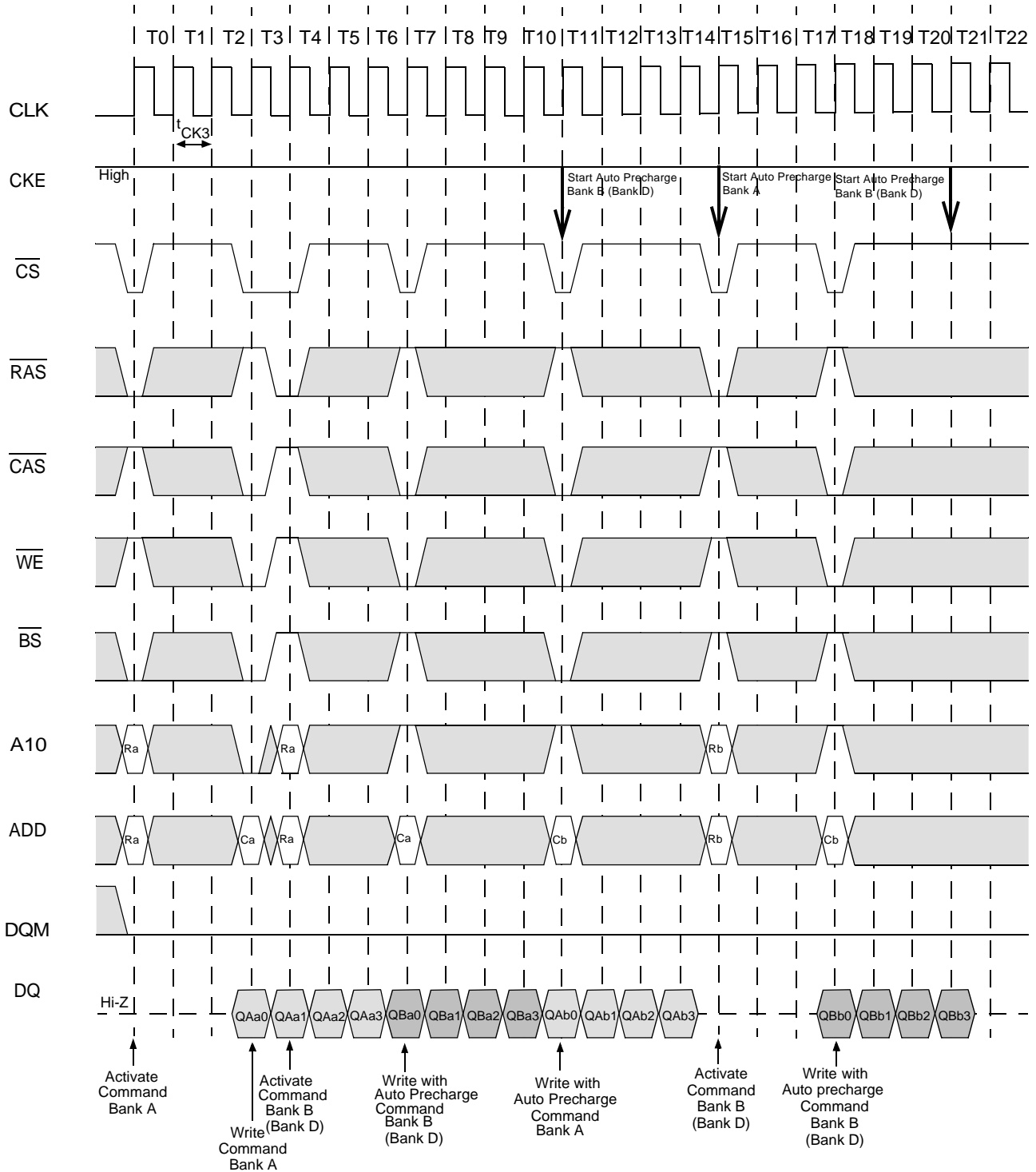
Auto Precharge after Write Burst (1 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2



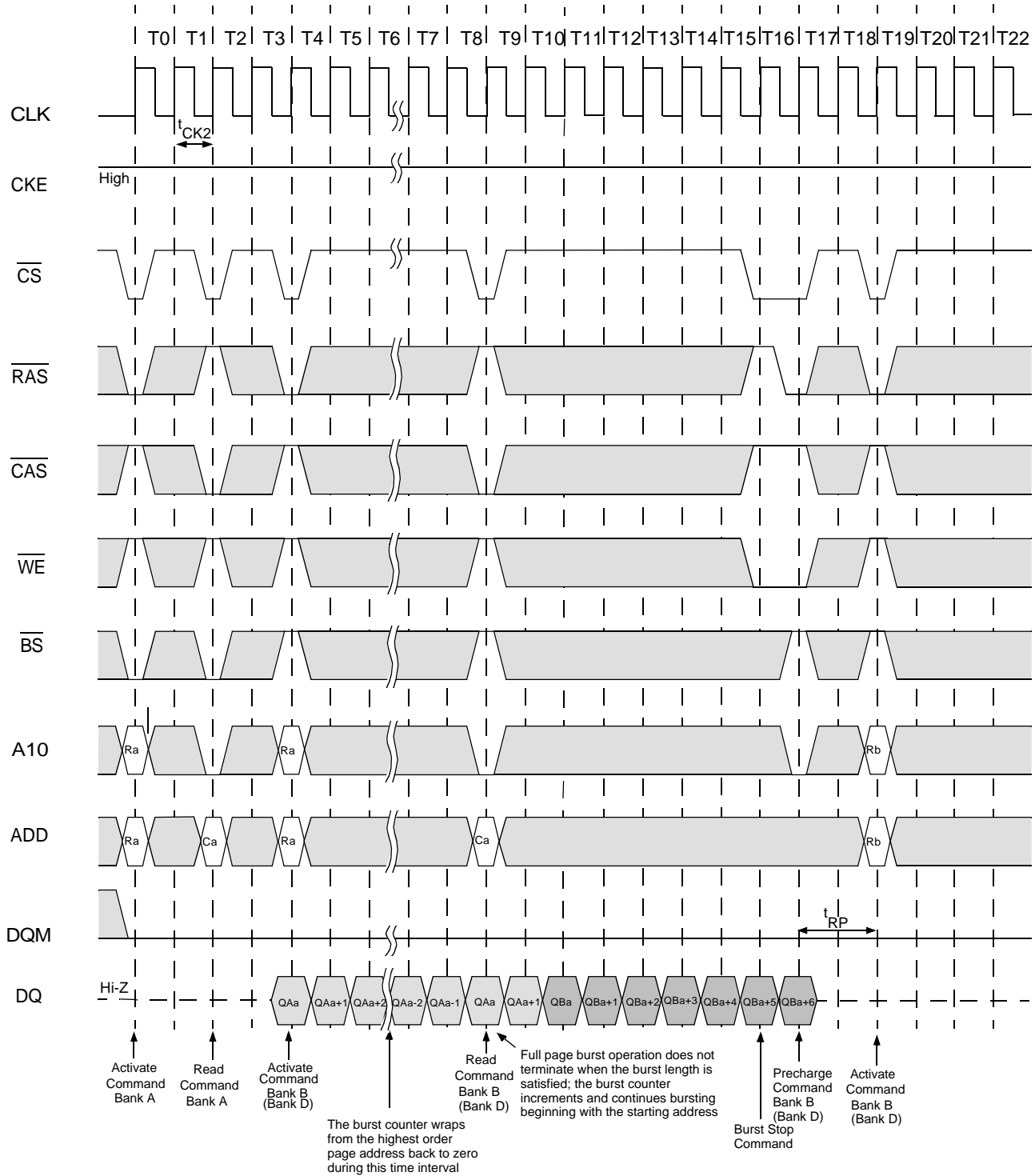
Auto Precharge after Write Burst (2 of 2)

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3



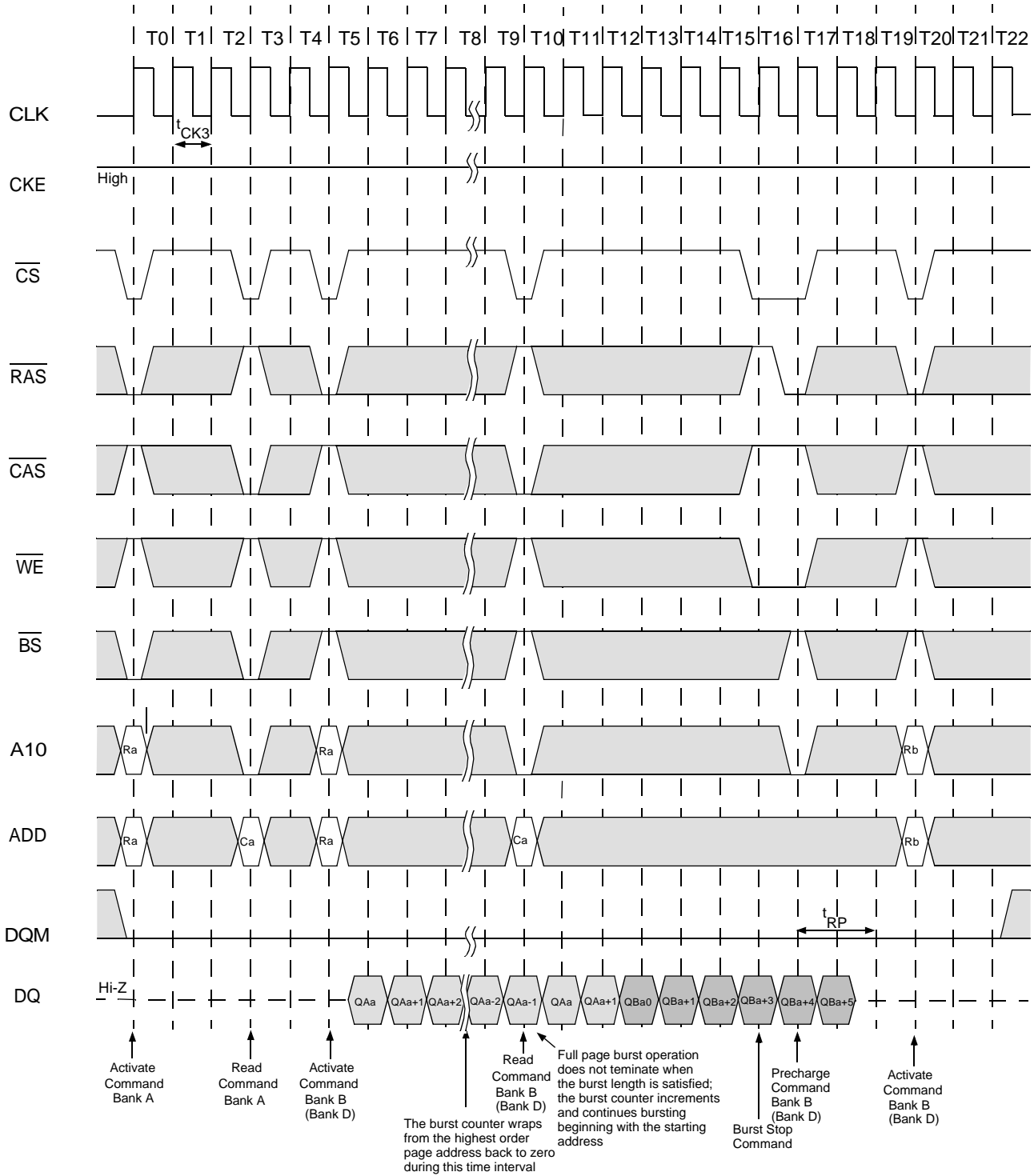
Full Page Read Cycle (1 of 2)

Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 2



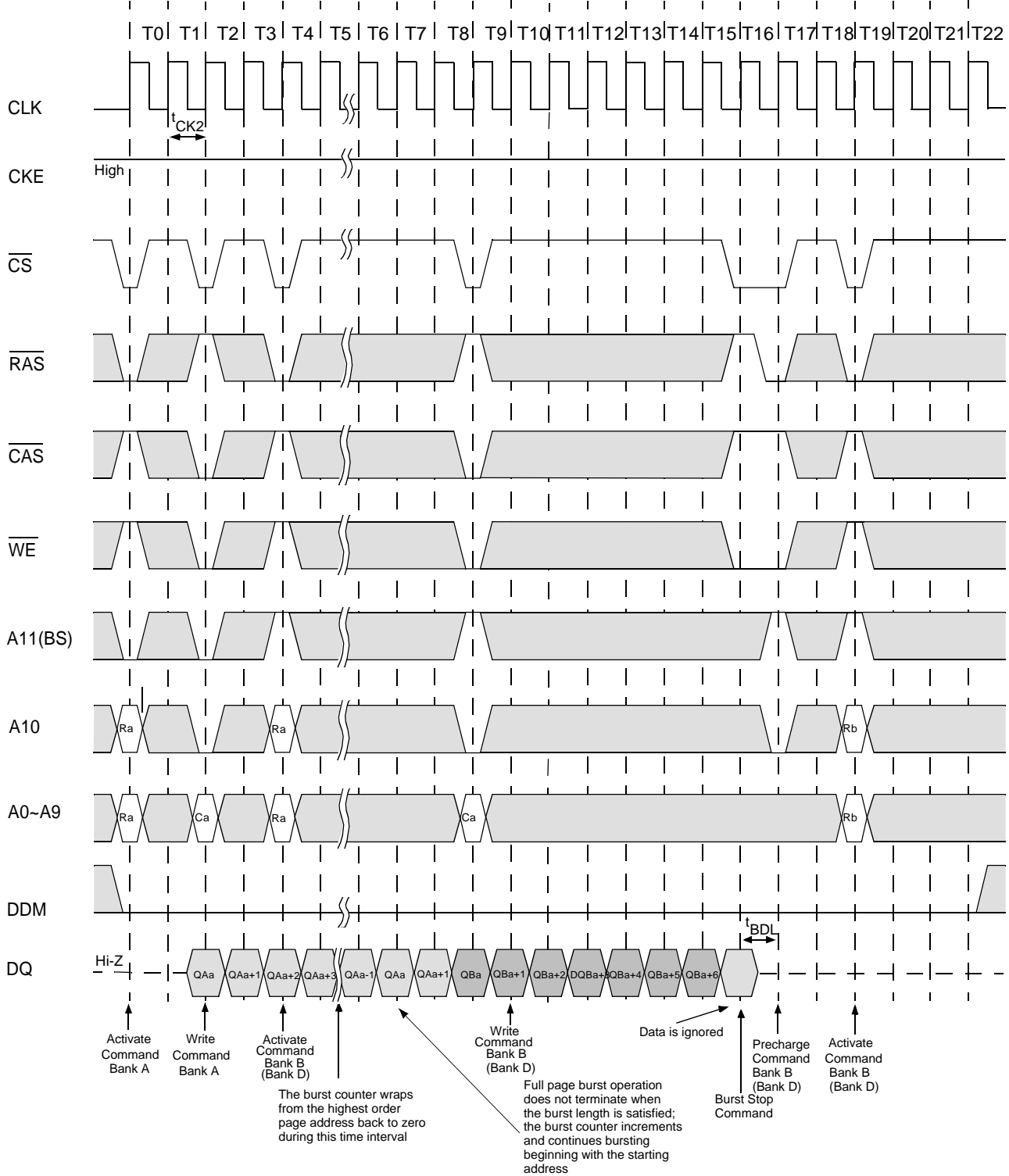
Full Page Read Cycle (2 of 2)

Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 3



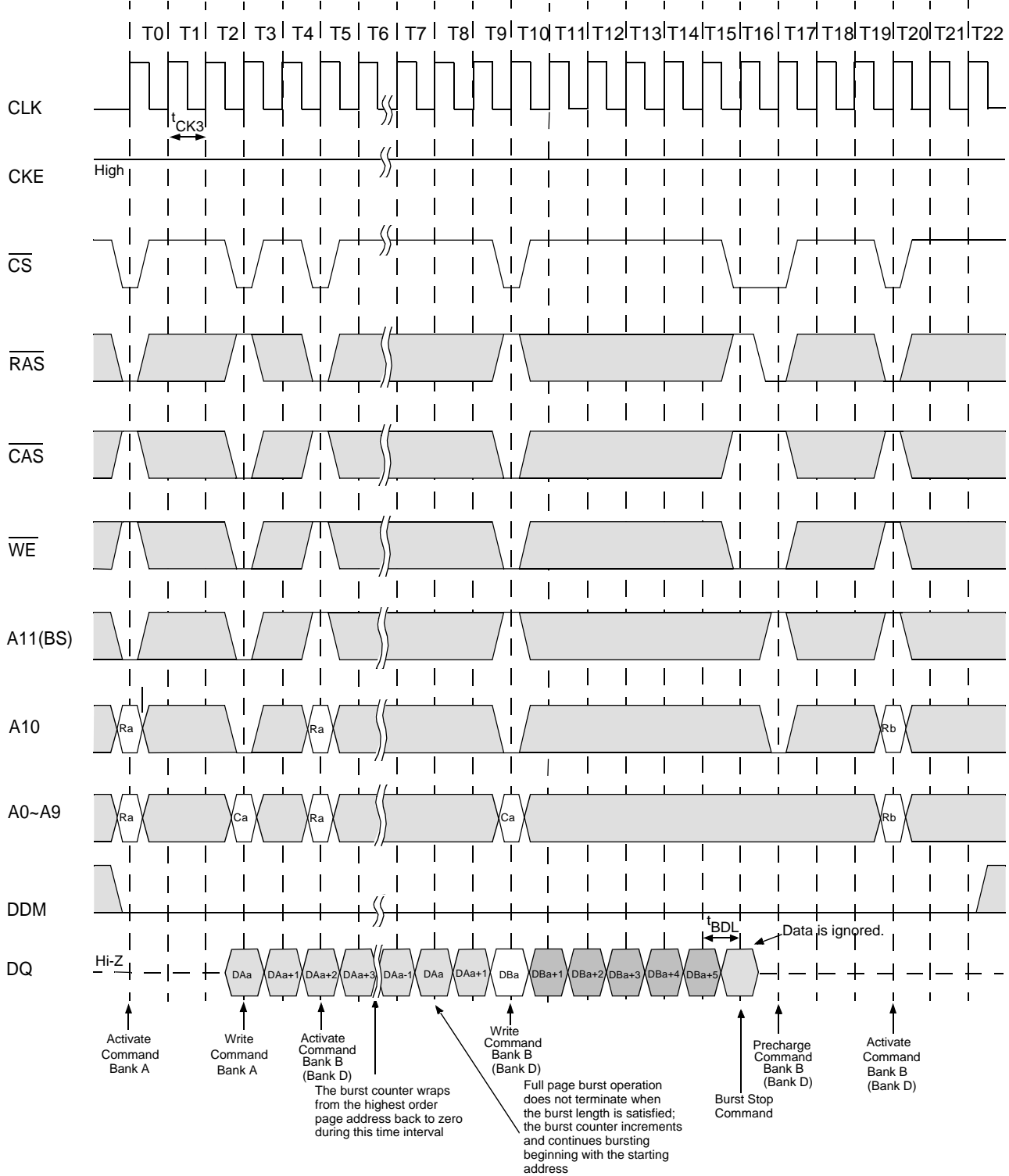
Full Page Write Cycle (1 of 2)

Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 2



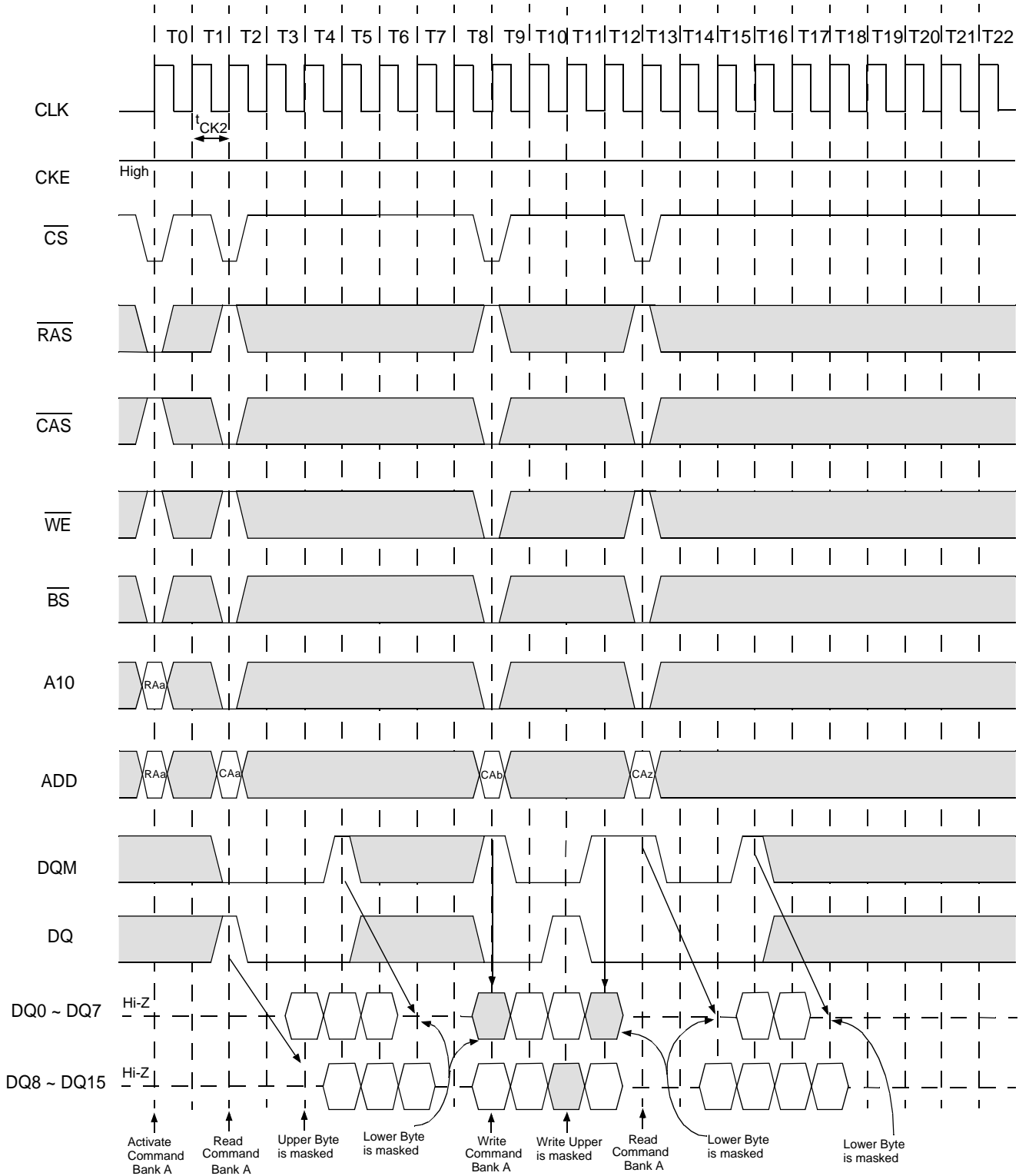
Full Page Write Cycle (2 of 2)

Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 3



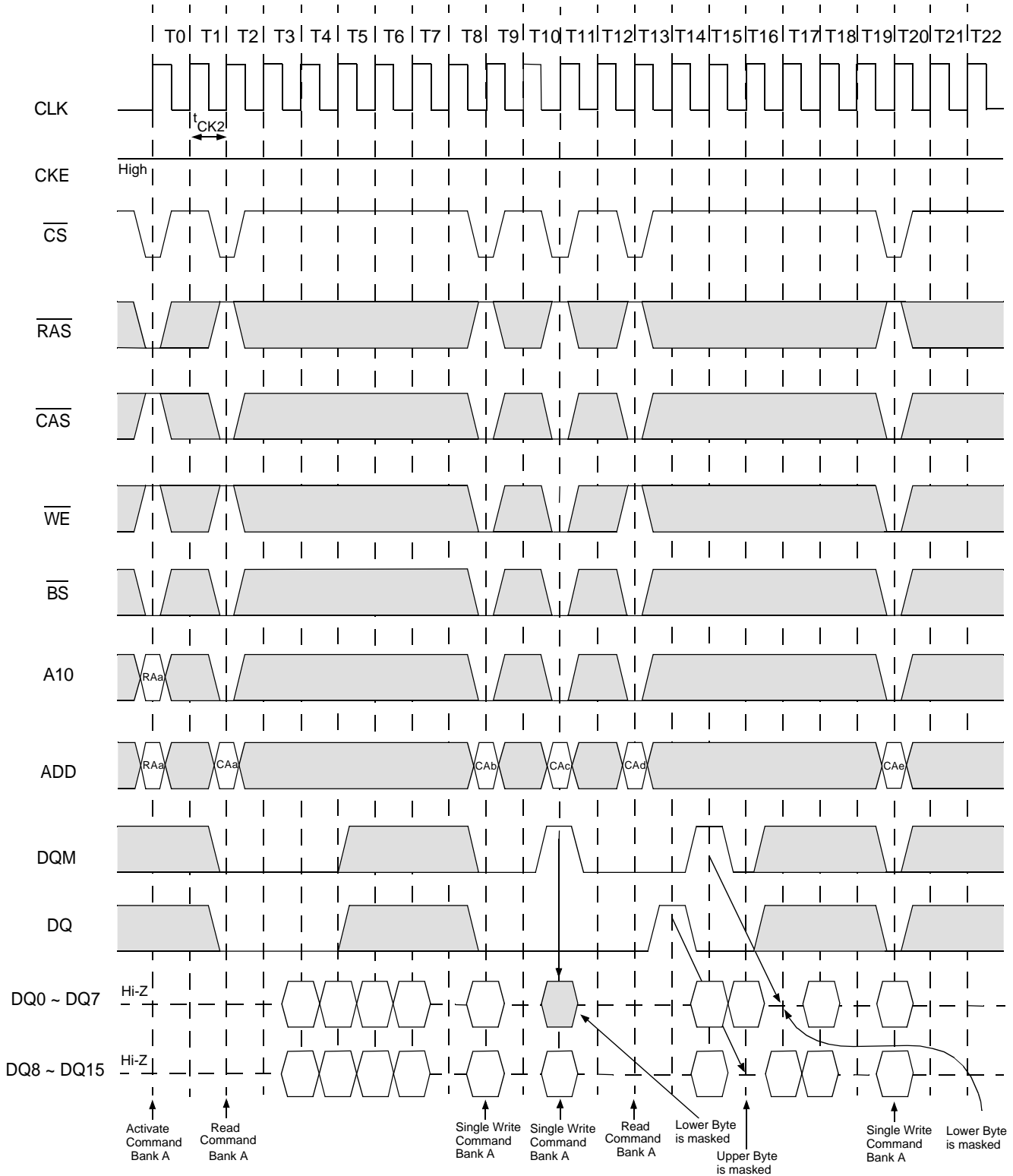
Byte Write Operation

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2



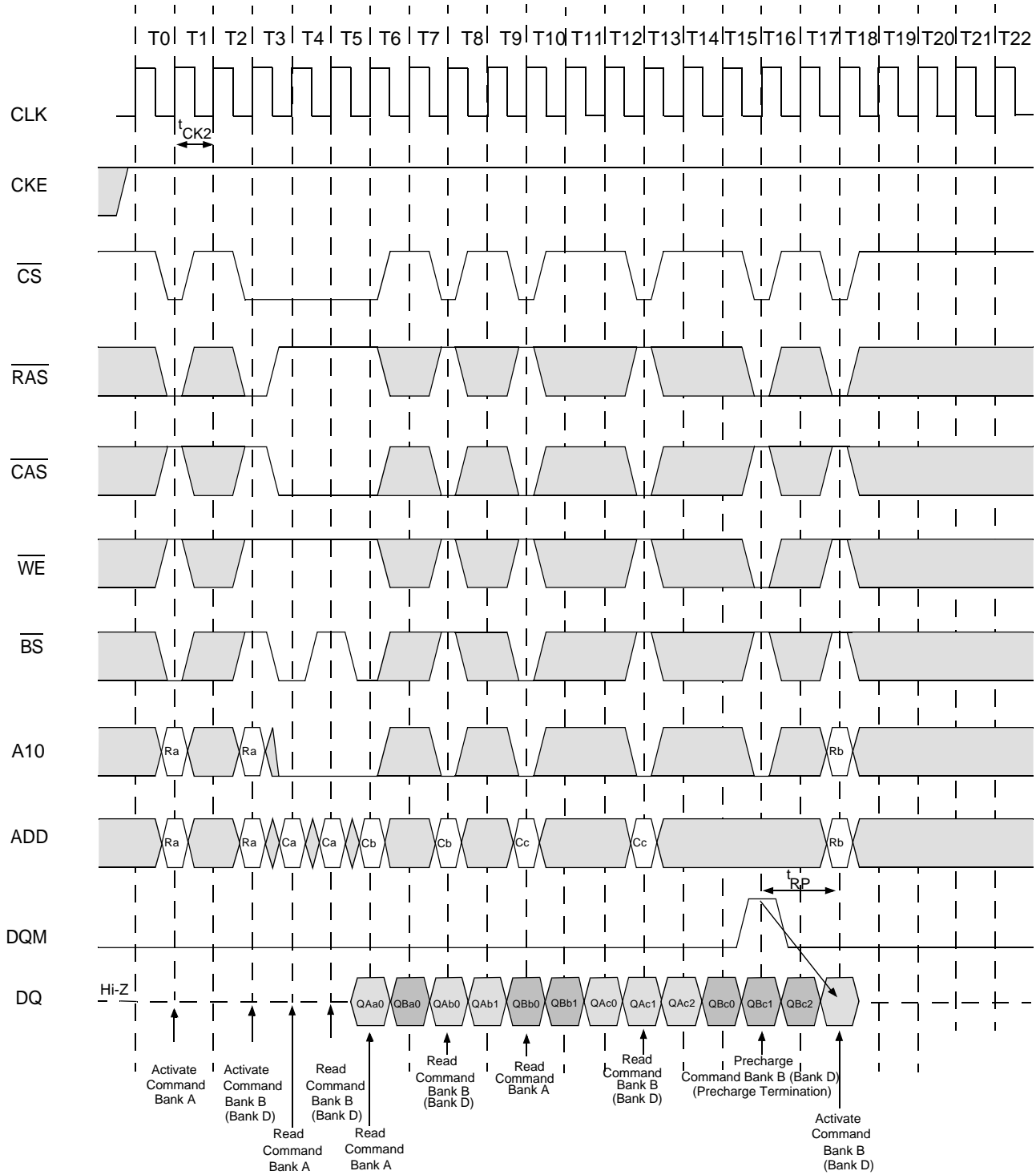
Burst Read and Single Write Operation

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2



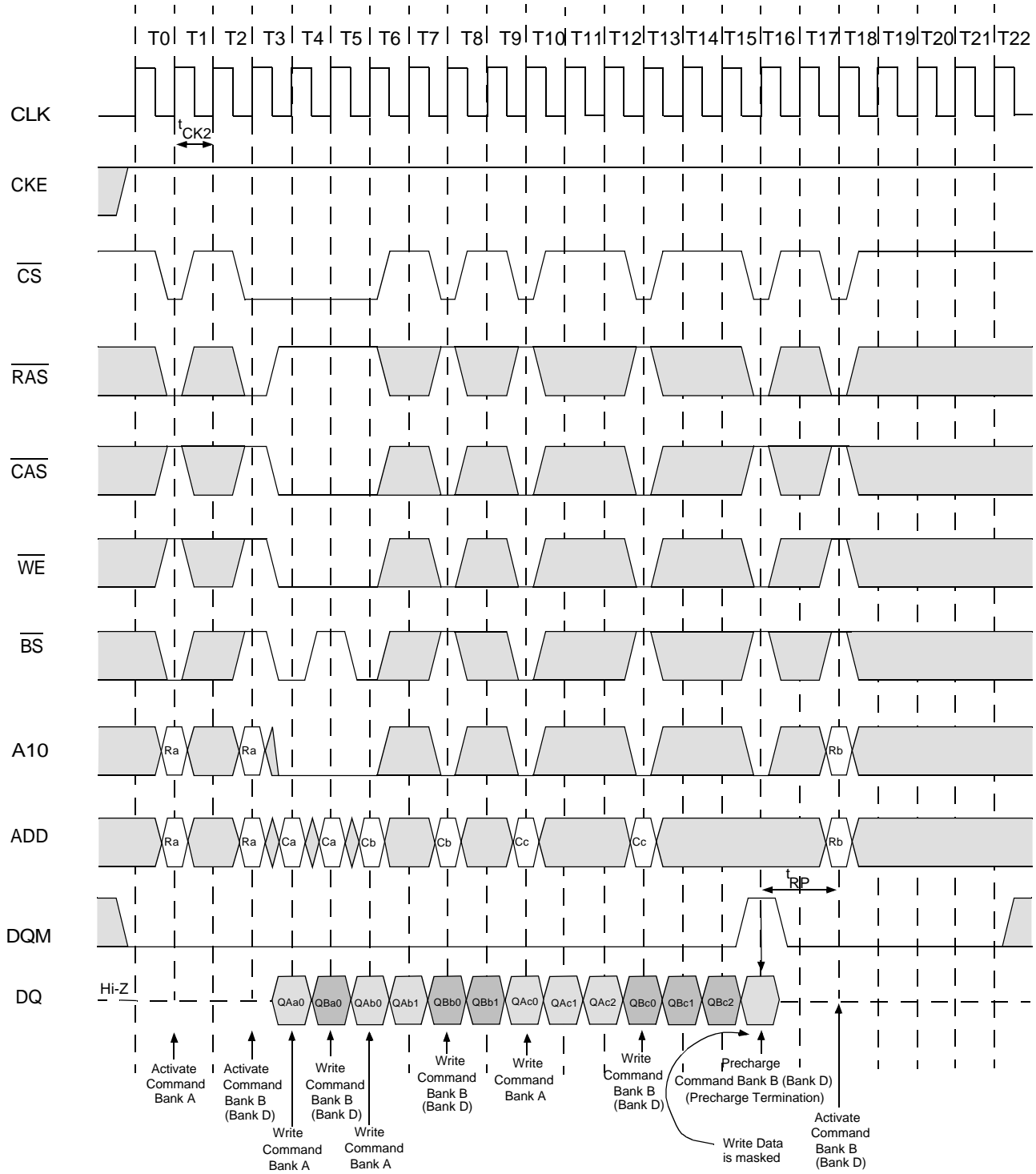
Full Page Random Column Read

Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 2



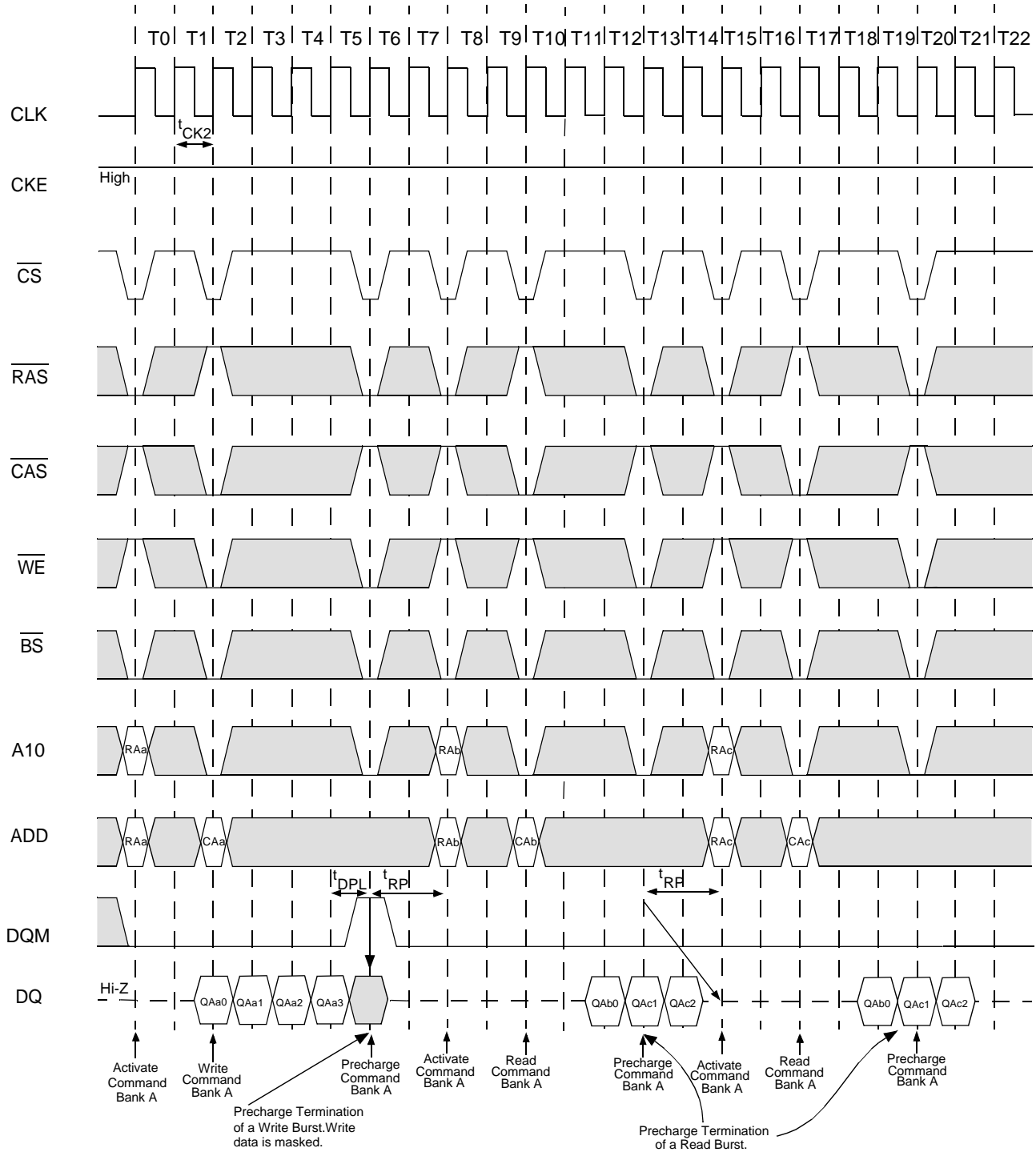
Full Page Random Column Write

Burst Length = Full Page, CAS Latency = 2



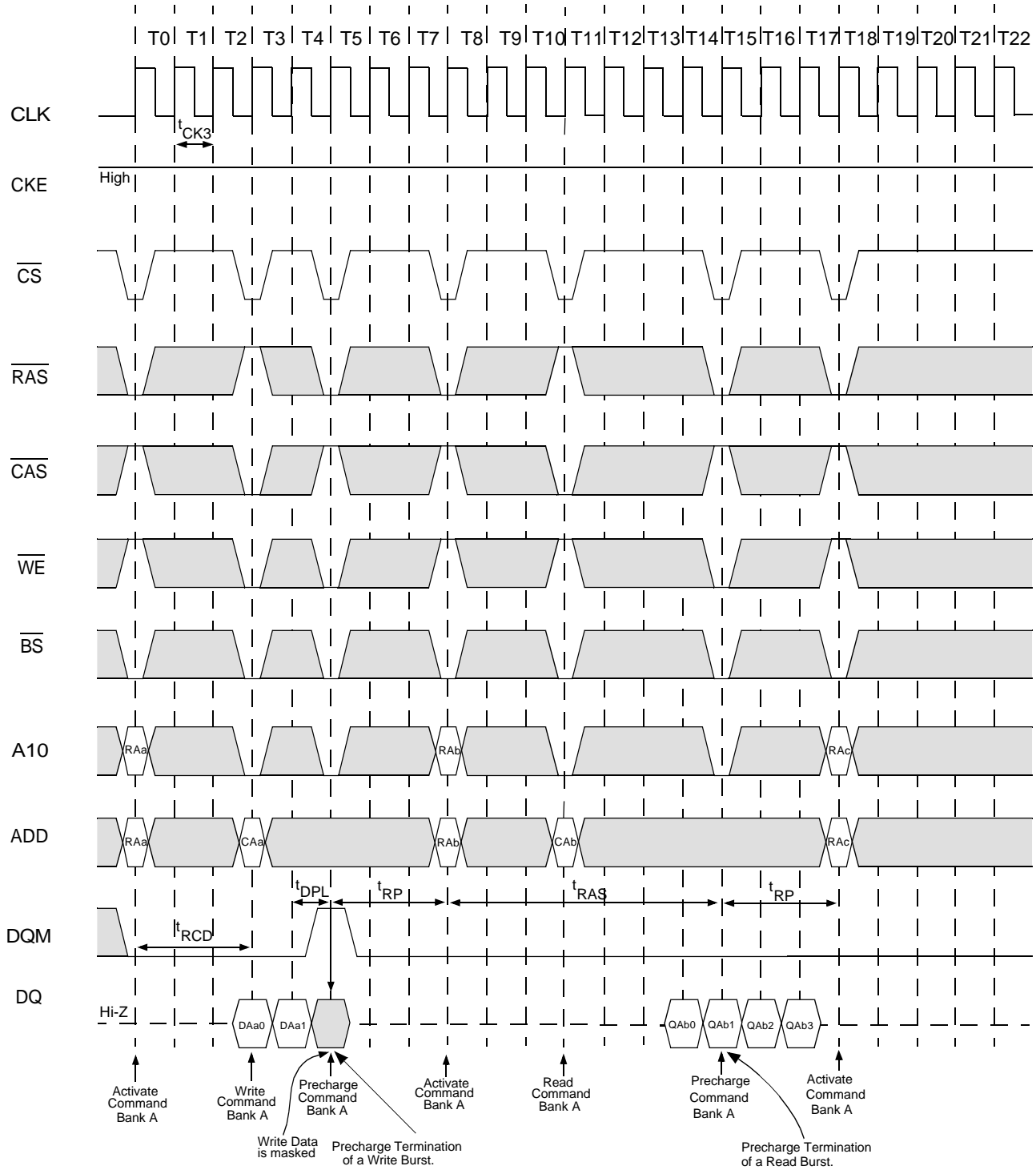
Precharge Termination of a Burst (1 of 2)

Burst Length = 4,8 or Full Page, CAS Latency = 2



Precharge Termination of a Burst (2 of 2)

Burst Length=4,8 or Full Page, $\overline{\text{CAS}}$ Latency=3



Ordering information

Part Number	Cycle time	Package
VG36643241BT-7	7ns	400mil 44-Pin Plastic TSOP
VG36643241BT-8	8ns	
VG36643241BT-10	10ns	

VG36643211BT-8

- VG → • VIS Memory Product
- 36 → • Technology/Design Rule
- 64 → • 64Mb
- 32 → • Device Configuration, 32 : x32
- 1 → • Device Internal Banks, 1 : 2banks, 4 : 4banks
- 1 → • Interface Type, 1 : LVTTTL, 2 : SSTL-3
- B → • Mask/Design Version
- T → • Package Type, T : TSOP
- 8 → • Cycle time, 10 : 10ns, 8 : 8ns, 7 : 7ns

Packaging Information

- 400mil, 86-Pin Plastic TSOP

